Appendix G - ZX-1280 Series Hardware Reference

The ZX-1280 series devices utilize the 100-pin TQFP package version of the Atmel AVR ATmega1280 microcontroller that has been programmed with the ZX control firmware. In order to use the ZX-1280 or ZX-1280n you must add several additional components as described below. In each of the diagrams presented below, only a portion of the ZX pins is shown. Those that are not germane to the circuit being discussed are omitted for clarity.

G.1 ZX-1280 Series Specifications

The electrical specifications of the ZX-1280 series devices are exactly those of the ATmega1280. Rather than reproducing them here the reader is directed to the datasheet published by Atmel. It can be obtained from the Atmel website http://www.atmel.com or from the ZBasic website

http://www.zbasic.net.

Non volatile data memory 4064 bytes
Program memory 124K

User Ram 8K

The memory spaces in the AVR architecture are all linear and regular memory maps. Program Flash memory space is divided in two sections, the Boot Program section and the Application Program section. Both sections have dedicated Lock bits for write and read/write protection. The SPM instruction that writes into the Application Flash memory section must reside in the Boot Program section.

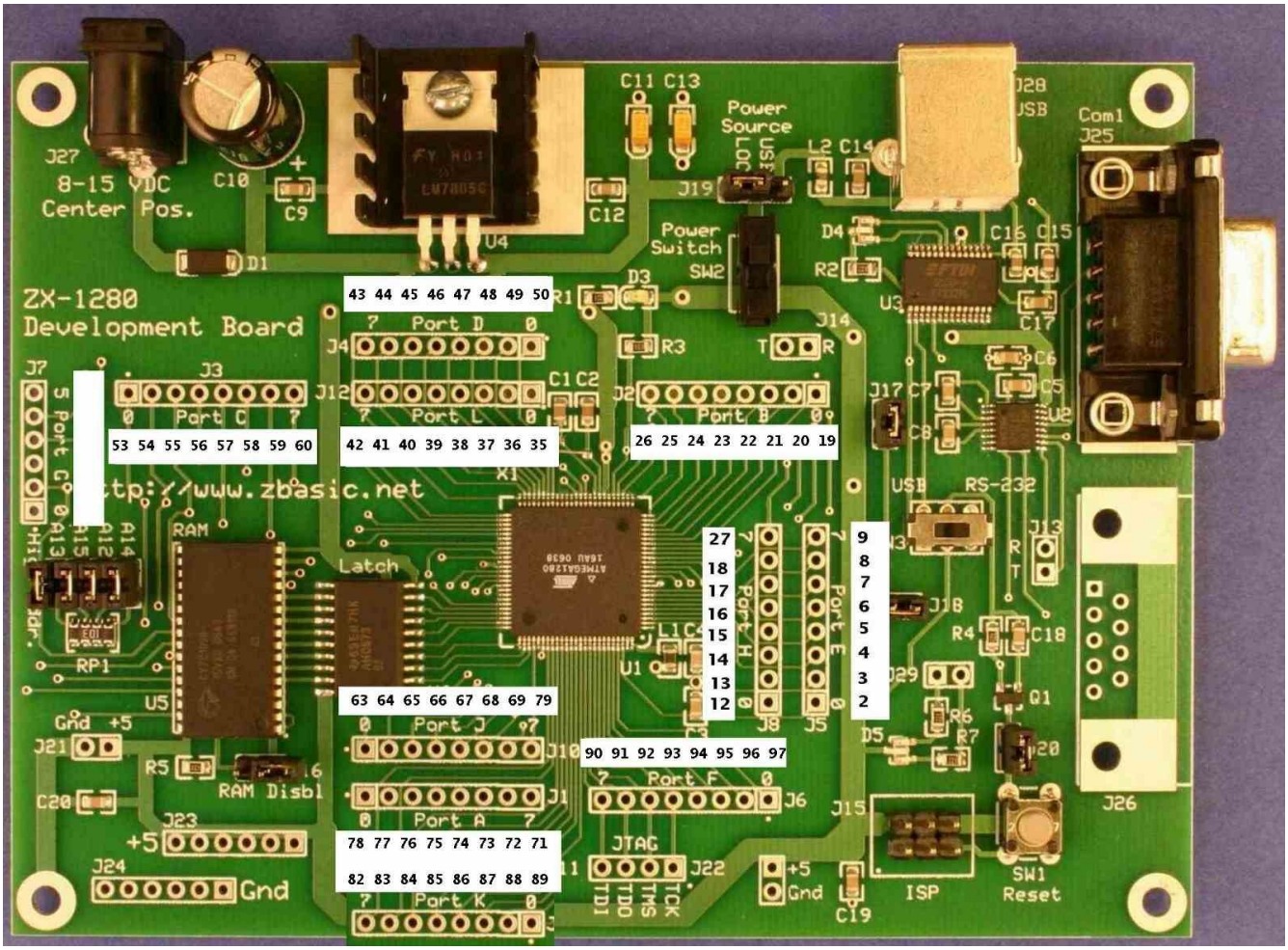
The ATmega1280 contains 64K bytes On-chip In-System Reprogrammable Flash memory for program storage, see Table 3 on page 19.

Since all AVR instructions are 16 or 32 bits wide, the Flash is organized as 64K x 16. For software security, the Flash Program memory space is divided into two sections, Boot Program section and Application Program section. The Flash memory has an endurance of at least 10,000 write/erase cycles. The ATmega1280 Program Counter (PC) is 16 bits wide, thus addressing the 64K program memory locations. The operation of Boot Program section and associated Boot Lock bits for software protection are described in detail in “Boot Loader Support – Read-While-Write Self-Programming” on page 323 of the AVR Atmega 1280 Data sheet.

“Memory Programming” on page 342 contains a detailed description on Flash data serial downloading using the SPI pins or the JTAG interface.

ZX-1280n Technical Features[1]

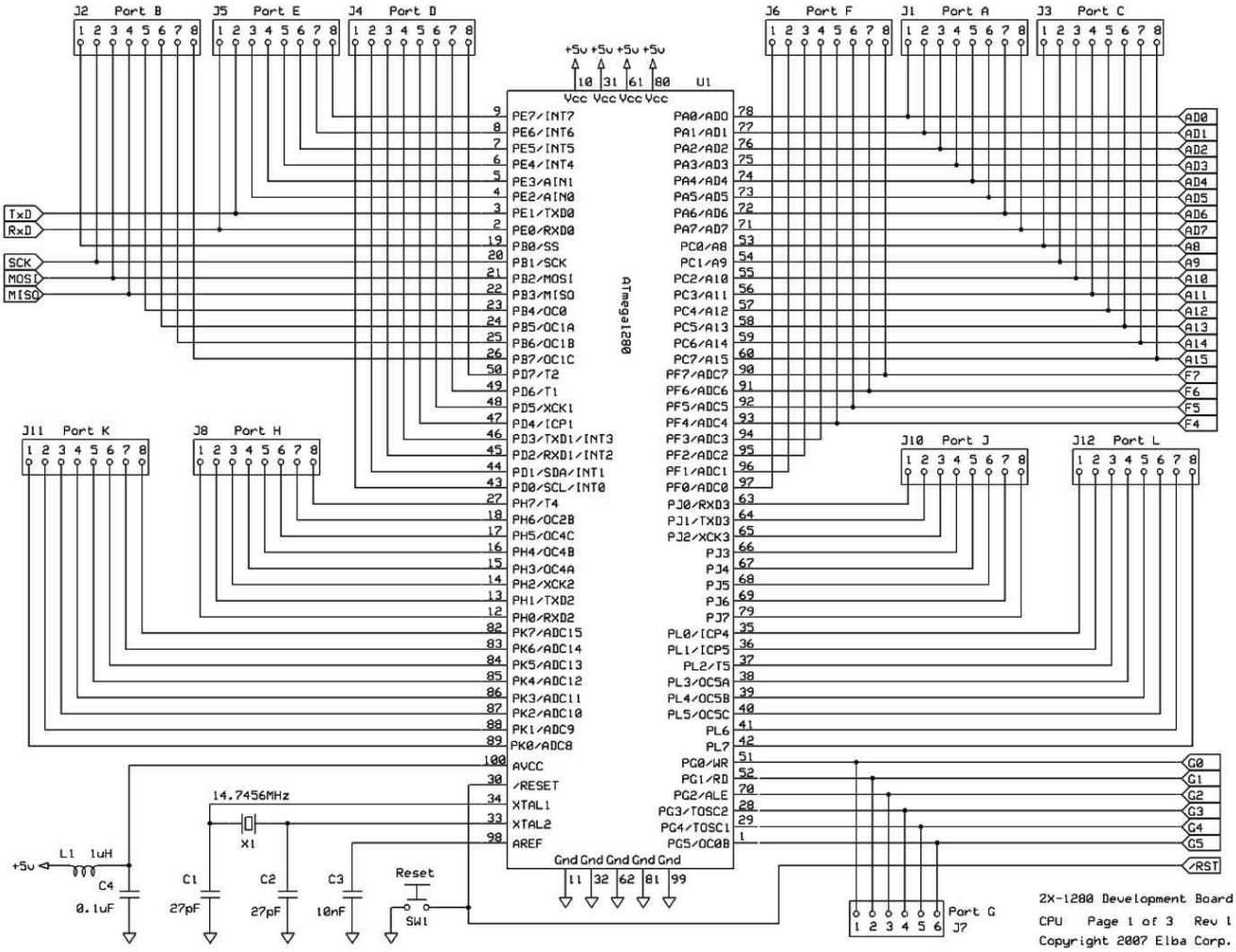
Package	100-pin TQFP
Operating Temperature	-40 to +85°C
Processor	Atmel AVR ATmega1280
Power Requirements	4.5 to 5.5VDC regulated at 200mA
Processor Speed	Up to 14.7MIPS (14.7MHz)
Program Execution Speed	**Up to 2.9 million instructions/sec[2]**
User RAM - standard	8K bytes
User RAM - maximum	63K bytes
Non-volatile Data Memory	4064 bytes
Program Memory	**124K bytes**
Digital I/O pins	86[3]
PWM Channels	Up to 12 channels, 16-bit resolution
Analog-to-Digital Channels	Up to 16 channels, 10-bit resolution
I2C Support	1 HW channel, 4 SW channels
1-Wire Support	Bit and byte level
SPI Support	4 HW channels
Synchronous Serial I/O Support	1 to 16 bits, MSB or LSB first
Asynchronous Serial I/O Ports	4-HW, up to 4 SW full duplex
X-10 Command Support	Yes
Multi-tasking Support	Yes
External Interrupts	Up to 30
Analog Comparator Interrupt	Yes
Interval Timer	Yes
Exception Handling Support	Yes
Floating Point Math	Yes - IEEE 32-bit
Advanced Floating Point Functions (sin, cos, log, etc.)	System Level
Programming Interface	Serial - 115.2K baud
Field Upgradeable System Software	**No**
Supports Inline Assembly	**Yes**
Supports Interrupt Handling Code	**Yes**



ZX-1280, ZX-1280n

Output Pins for 16-bit PWM Channel Numbers

Channel Numbers	1	2	3	4	5	6
Pin # Port Bit #	24 B 5	25 B 6	26 B 7	5 E 3	6 E 4	7 E 5
Channel Numbers	7	8	9	10	11	12
Pin # Port Bit #	15 H 3	16 H 4	17 H 5	38 L 3	39 L 4	40 L 5



Port A (PA7..PA0) Port A is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port A output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port A pins that are externally pulled low will source current if the pull-up resistors are activated. The Port A pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port A also serves the functions of various special features of the ATmega1280 as listed on page 91.

Port B (PB7..PB0) Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B has better driving capabilities than the other ports.
Port B also serves the functions of various special features of the Atmega 1280 as listed on page 92.

Port C (PC7..PC0) Port C is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port C output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running.
Port C also serves the functions of special features of the ATmega1280 as listed on page 95.

Port D (PD7..PD0) Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.
Port D also serves the functions of various special features of the ATmega 1280 as listed on page 97.

Port E (PE7..PE0) Port E is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port E output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port E pins that are externally pulled low will source current if the pull-up resistors are activated. The Port E pins are tri-stated when a reset condition becomes active, even if the clock is not running.
Port E also serves the functions of various special features of the Atmega 1280 as listed on page 99.

Port F (PF7..PF0) Port F serves as analog inputs to the A/D Converter.
Port F also serves as an 8-bit bi-directional I/O port, if the A/D Converter is not used. Port pins can provide internal pull-up resistors (selected for each bit). The Port F output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port F pins that are externally pulled low will source current if the pull-up resistors are activated. The Port F pins are tri-stated when a reset condition becomes active, even if the clock is not running. If the JTAG interface is enabled, the pull-up resistors on pins PF7(TDI), PF5(TMS), and PF4(TCK) will be activated even if a reset occurs. Port F also serves the functions of the JTAG interface.

Port G (PG5..PG0) Port G is a 6-bit I/O port with internal pull-up resistors (selected for each bit). The Port G output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port G pins that are externally pulled low will source current if the pull-up resistors are activated. The Port G pins are tri-stated when a reset condition becomes active, even if the clock is not running.
Port G also serves the functions of various special features of the Atmega 1280 as listed on page 105.

Port H (PH7..PH0) Port H is a 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port H output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port H pins that are externally pulled low will source current if the pull-up resistors are activated. The Port H pins are tri-stated when a reset condition becomes active, even if the clock is not running. Port H also serves the functions of various special features of the Atmega 1280 as listed on page 107.

Port J (PJ7..PJ0) Port J is a 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port J output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port J pins that are externally pulled low will source current if the pull-up resistors are activated. The Port J pins are tri-stated when a reset condition becomes active, even if the clock is not running. Port J also serves the functions of various special features of the Atmega 1280 as listed on page 109.

Port K is a 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port K output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port K pins that are externally pulled low will source current if the pull-up resistors are activated. The Port K pins are tri-stated when a reset condition becomes active, even if the clock is not running.
Port K also serves the functions of various special features of the ATmega1280 as listed on page 111.

Port L (PL7..PL0) Port L is a 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port L output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port L pins that are externally pulled low will source current if the pull-up resistors are activated. The Port L pins are tri-stated when a reset condition becomes active, even if the clock is not running.
Port L also serves the functions of various special features of the ATmega1280 as listed on page 113.

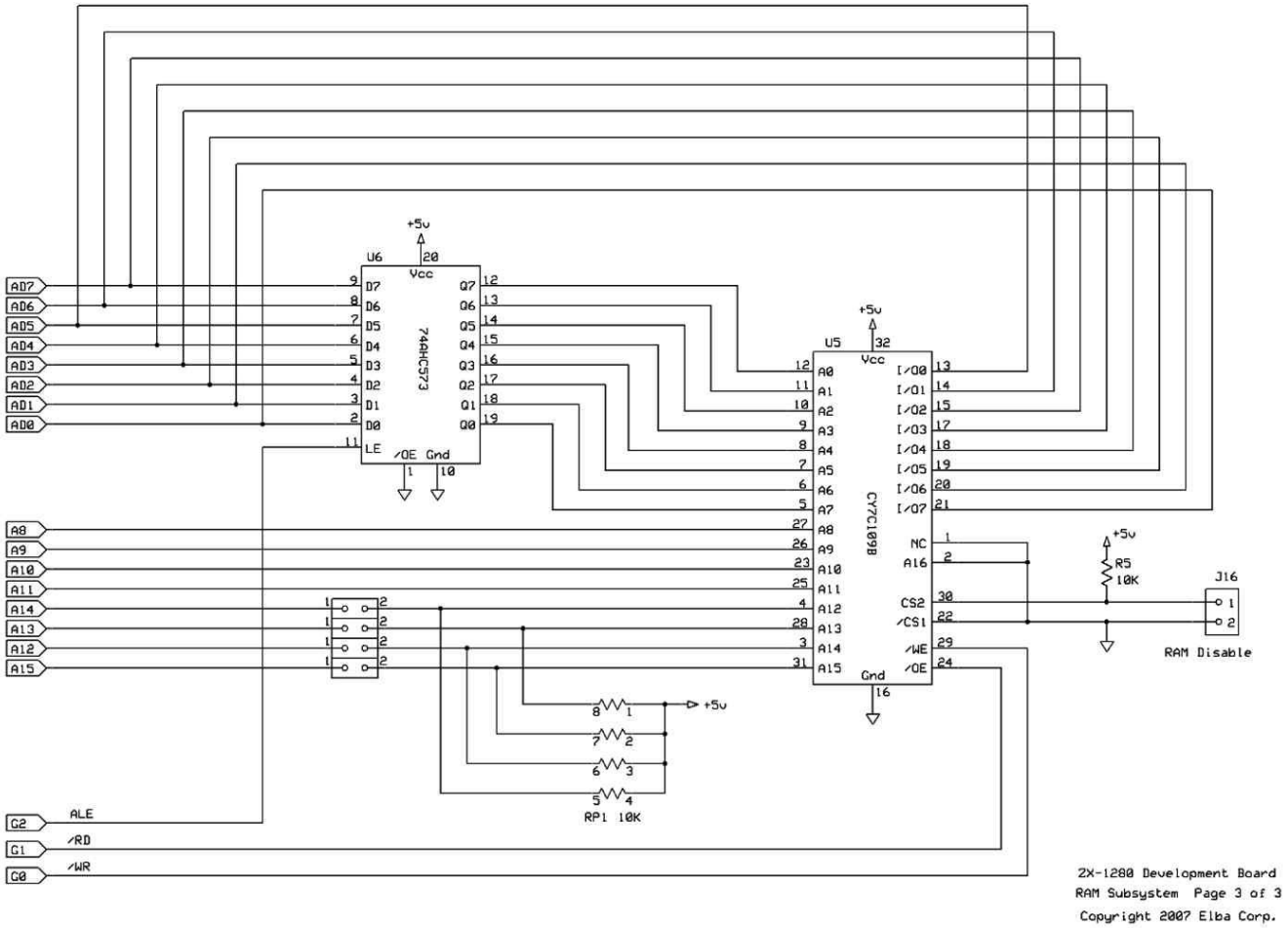
RESET Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. The minimum pulse length is given in Table 26 on page 58. Shorter pulses are not guaranteed to generate a reset.

XTAL1 Input to the inverting Oscillator amplifier and input to the internal clock operating circuit.

XTAL2 Output from the inverting Oscillator amplifier.

AVCC AVCC is the supply voltage pin for Port F and the A/D Converter. It should be externally connected to VCC, even if the ADC is not used. If the ADC is used, it should be connected to VCC through a low-pass filter.

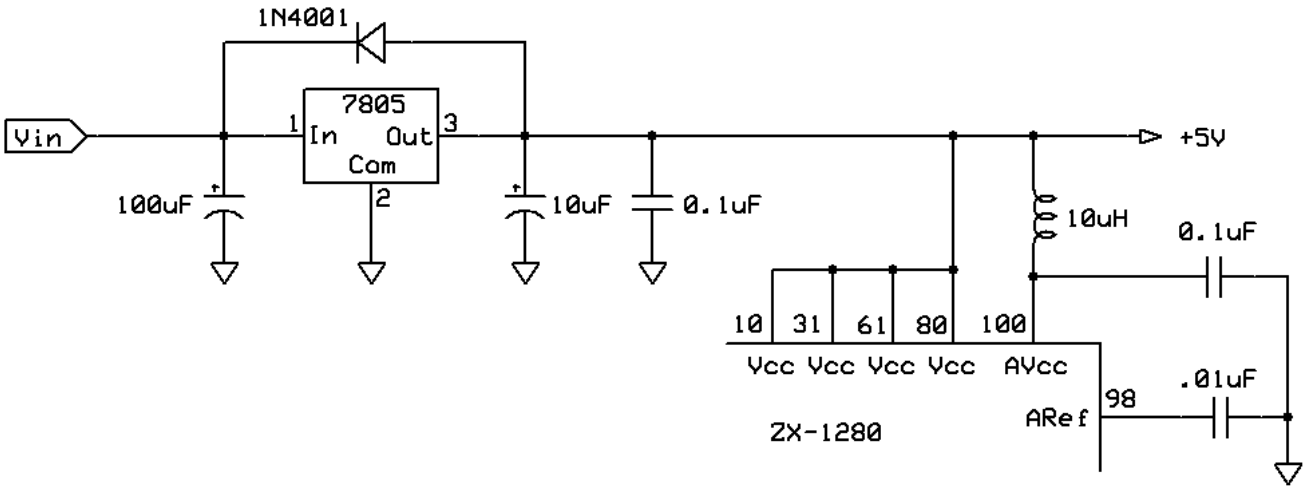
AREF This is the analog reference pin for the A/D Converter.



G.2 ZX-1280 Series Devices Required External Components

The circuits described below represent the minimum external circuitry required to operate the ZX-1280 or ZX-1280n. Depending on your application, you may need additional circuitry to take advantage of the capabilities of the ZX-1280 series device. In contrast to some other ZX devices, the ZX-1280 series does not require an external EEPROM for program storage. Rather, the compiled user program is stored in the ZX's internal Flash memory. The maximum user program size is 60K bytes for the ZX-1280 and 124K for the ZX-1280n.

Power Source



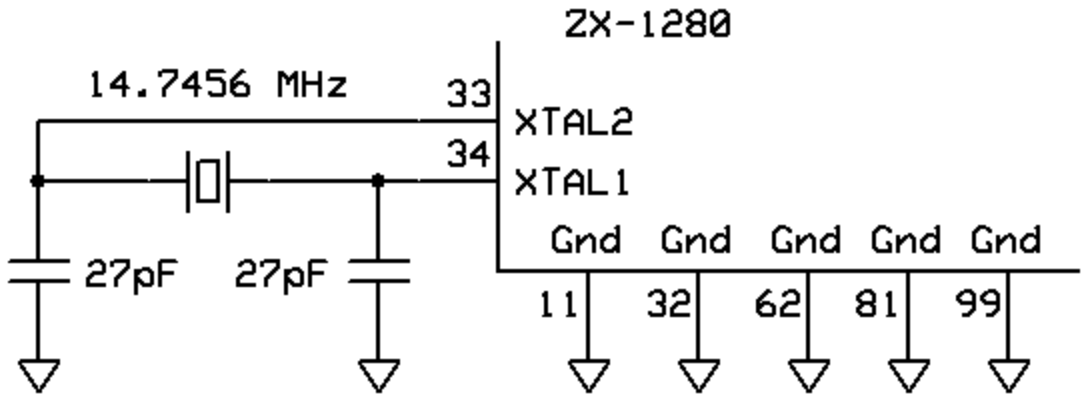
The ZX-1280 series devices need a regulated voltage source capable of providing at least 200mA of current. The voltage typically used is 5 volts but the ZX-1280 will operate between 4.5 volts and 5.5 volts. A recommended circuit is shown below. A suitable heatsink will probably be required in most cases to keep the regulator IC below its maximum operating temperature. Consult the regulator datasheet for more information.

ZX-1280 Series Power Source

If you do not plan to use the Analog-to-Digital converter channels you can eliminate the inductor and the two capacitors on the right side of the diagram. In this case, pin 64 would be connected directly to the power source (same as pin 21, etc.) and pin 62 can be left open. Although not shown on this diagram, the ground pins of the ZX-1280 (pins 11, 32, 62, 81 and 99) must be connected to the common ground of the system.

Clock Source

The ZX-1280 series devices require a clock source running at 14.7456MHz. The easiest way to provide this clock source is to connect a crystal of that frequency to pins 33 and 34 along with the necessary capacitors.
The recommended crystal to use is ECS-147.4-20-4 (Digi-Key #X175-ND). Alternate crystals are the ECS-147.4-20-1 (Digi-Key #X142-ND) in a slightly larger package and the ECS-147.4-18-9 (Digi-Key #XC-957ND) in a cylindrical package. The capacitor value to use depends somewhat on the layout (e.g. stray capacitance). Values in the range of 22pF to 27pF have been used successfully in various situations.



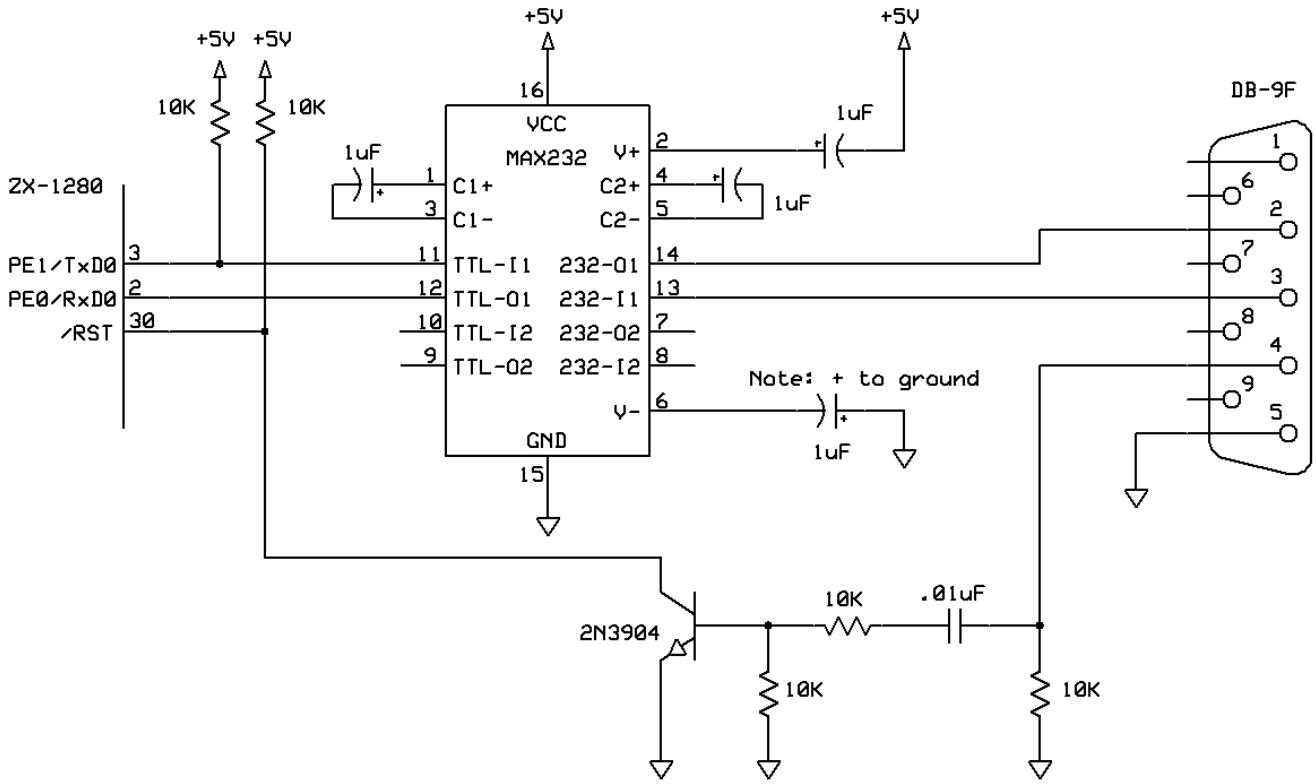
If you already have a clock source at the required frequency you can feed that signal directly to pin 34. In this case there would be no connection to pin 33.

Serial Interface

The ZX-1280 series devices require a serial interface for downloading code into Program Memory, performing field updates of the control program, and for your program's use via Com1. The recommended serial interface circuitry is shown below. This circuit has two sub components. The MAX232 chip functions as an RS-232 level converter that translates the 0-5 volt signals of the ZX to the standard RS-232 voltage levels.

The second component is the ATN circuitry that is used to signal the ZX to go into download mode. The latter circuitry is that portion connected between pin 4 of the DB-9 serial connector and pin 30 of the ZX-1280. You may want to include a jumper in the ATN circuitry so that it can be disconnected when downloads are not required. With the ATN circuitry connected, the ZX will receive a reset pulse on every positive transition of pin 4 (DTR) of the serial connector. If alternate component values are chosen you must ensure that the ZX receives a reset pulse of at least 2uS on every positive transition of the DTR signal on pin 4 of the serial connector.

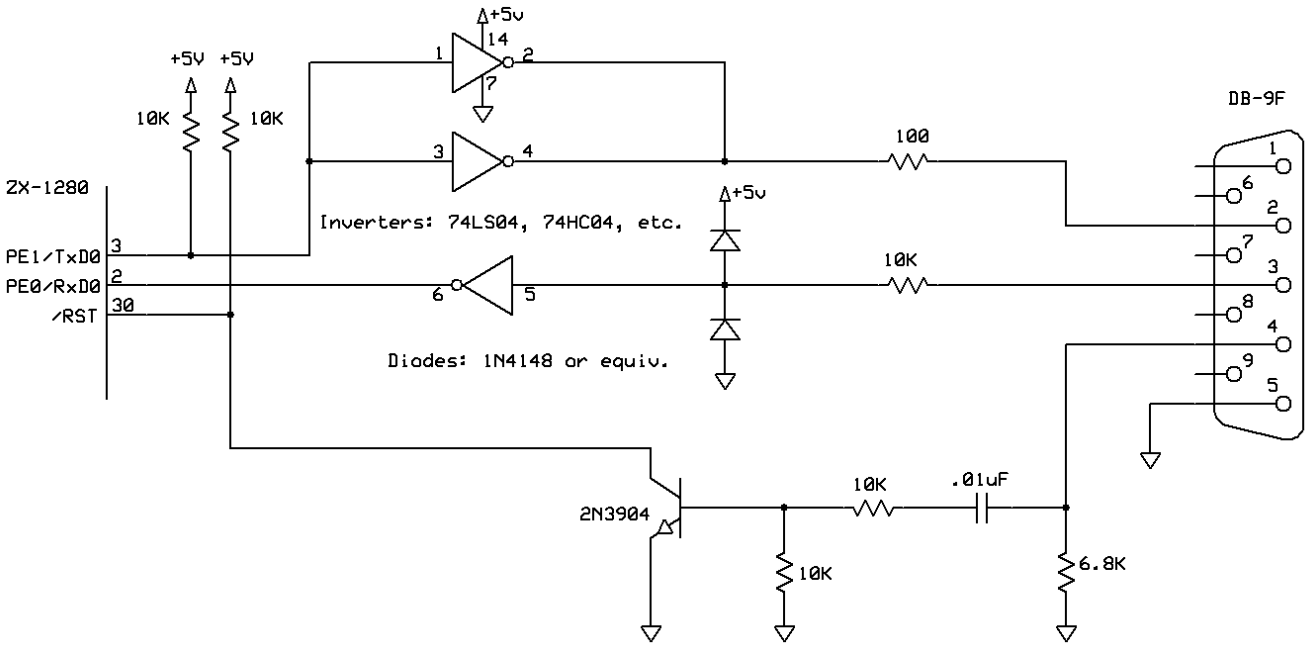
One advantage to using this recommended circuit is that the MAX232 chip includes a DC-DC converter that produces nominally +/- 12V from the 5 volt source. This is particularly useful if your application requires one or more of these voltages. For example, some LCD devices require a low-current negative supply for their backlight circuitry. The positive voltage is available on pin 2 of the MAX232 while the negative voltage is available on pin 6. Consult the datasheet for the MAX232 device for information on the current capacity of these supplies.



Recommended ZX-1280 Series Serial Interface Circuit

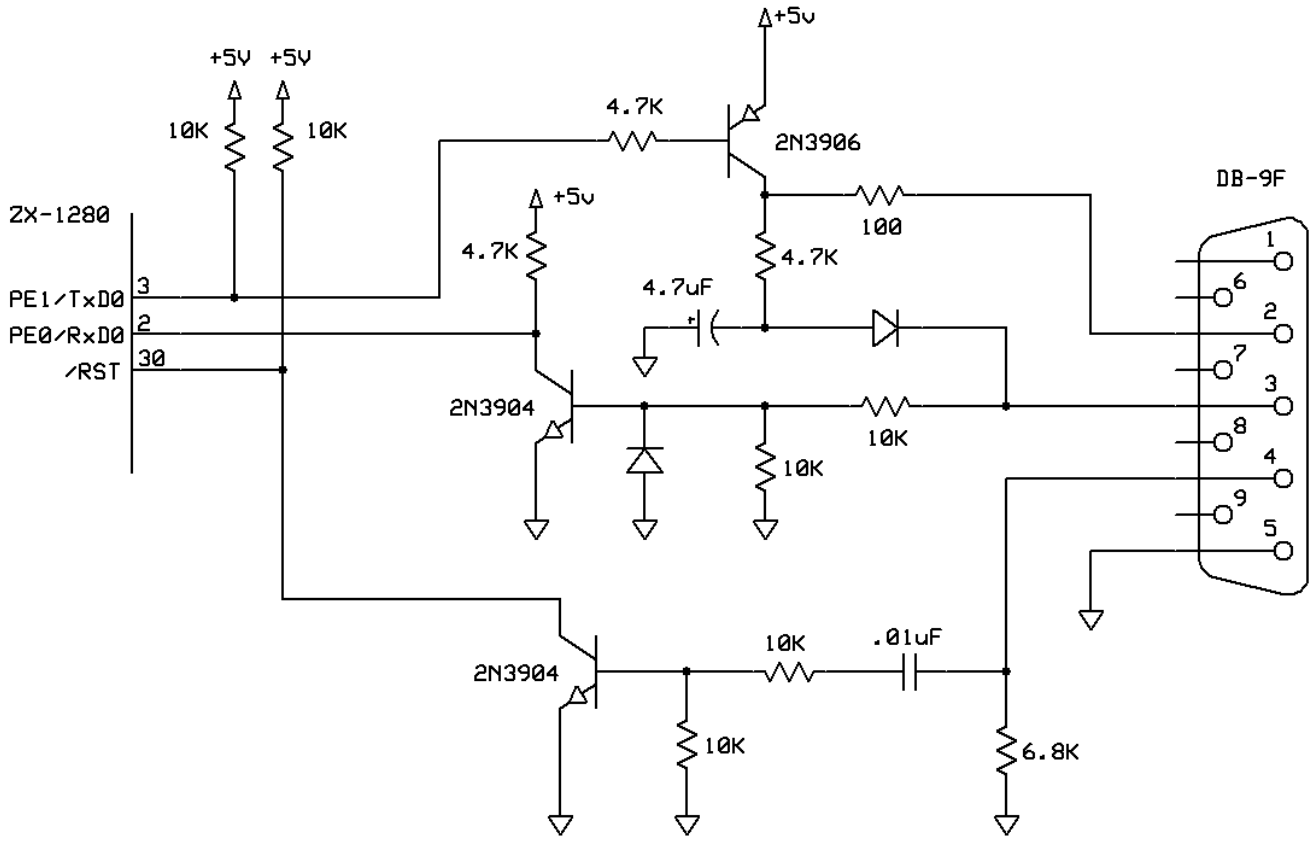
The pullup resistor shown on the ZX's Com1 transmit output (pin 28) is needed to ensure that the serial output line stays in the idle state during reset cycles. Its value is non-critical – anything from 4.7K to 22K should work fine. The pullup resistor on the reset input isn't technically required since the chip itself has an internal pullup. The external pullup could be eliminated or could be made larger if desired.

There are other serial interface circuits that would provide the required functionality, two of which are shown below. Both alternate circuits use the same ATN circuitry as the recommended circuit above.



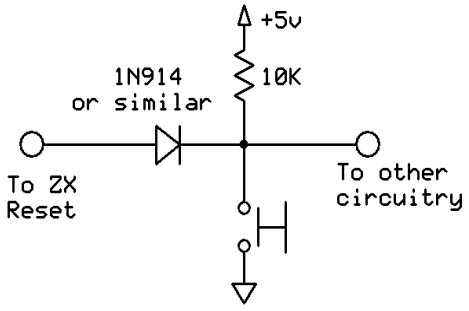
The first alternate above is similar to the circuitry used on the ZX-24 series devices. The advantage to this circuit is its simplicity. The disadvantage is that the voltage levels of the serial output signal do not meet the RS-232 standard. Even so, most serial receivers are able to properly interpret the output signal. Note that if the inverters used have protection diodes on their inputs the external diodes shown are not necessary.

The second alternate serial interface is shown in the diagram below. This circuit produces a serial output signal that meets the RS-232 standard by using the negative voltage on the receive line to provide a reference for the output level. Although the parts count is higher, the circuit uses inexpensive and non-critical components.



Reset Circuit

You may also want to incorporate a reset button in your circuitry. If so, a normally open, momentary contact switch may be connected directly between pin 20 of the ZX and ground. If other circuitry in your application also needs the reset signal, you may want to isolate that circuitry from the ATN resets using a buffer gate or a diode. A suggested diode isolation circuit for the reset line is shown below.



Reset Signal Isolation