A Register Quick Reference

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
The Cortex-M3 Processor															
R0, type R/W, , reset - (see page 85)															
DATA															
DATA															
R1, type R/W, , reset - (see page 85)															
DATA															
DATA															
R2, type R/W, , reset - (see page 85)															
DATA															
DATA															
R3, type R/W, , reset - (see page 85)															
DATA															
DATA															
R4, type R/W, , reset - (see page 85)															
DATA															
DATA															
R5, type R/W, , reset - (see page 85)															
DATA															
DATA															
R6, type R/W, , reset - (see page 85)															
DATA															
DATA															
R7, type R/W, , reset - (see page 85)															
DATA															
DATA															
R8, type R/W, , reset - (see page 85)															
DATA															
DATA															
R9, type R/W, , reset - (see page 85)															
DATA															
DATA															
R10, type R/W, , reset - (see page 85)															
DATA															
DATA															
R11, type R/W, , reset - (see page 85)															
DATA															
DATA															
R12, type R/W, , reset - (see page 85)															
DATA															
DATA															
SP, type R/W, , reset - (see page 86)															
SP															
SP															
LR, type R/W, , reset 0xFFFF.FFFF (see page 87)															
LINK															
LINK															
PC, type R/W, , reset - (see page 88)															
PC															
PC															

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PSR, type R/W, , reset 0x0100.0000 (see page 89)															
N	Z	C	V	Q	ICI / IT		THUMB								
ICI / IT									ISRNUM						
PRIMASK, type R/W, , reset 0x0000.0000 (see page 93)															
															PRIMASK
FAULTMASK, type R/W, , reset 0x0000.0000 (see page 94)															
															FAULTMASK
BASEPRI, type R/W, , reset 0x0000.0000 (see page 95)															
								BASEPRI							
CONTROL, type R/W, , reset 0x0000.0000 (see page 96)															
														ASP	TMPL

Cortex-M3 Peripherals

System Timer (SysTick) Registers

Base 0xE000.E000

STCTRL, type R/W, offset 0x010, reset 0x0000.0004															
															COUNT
													CLK_SRC	INTEN	ENABLE
STRELOAD, type R/W, offset 0x014, reset 0x0000.0000															
								RELOAD							
RELOAD															
STCURRENT, type R/WC, offset 0x018, reset 0x0000.0000															
								CURRENT							
CURRENT															

Cortex-M3 Peripherals

Nested Vectored Interrupt Controller (NVIC) Registers

Base 0xE000.E000

EN0, type R/W, offset 0x100, reset 0x0000.0000
INT
INT
EN1, type R/W, offset 0x104, reset 0x0000.0000
INT
INT
DIS0, type R/W, offset 0x180, reset 0x0000.0000
INT
INT
DIS1, type R/W, offset 0x184, reset 0x0000.0000
INT
INT
PEND0, type R/W, offset 0x200, reset 0x0000.0000
INT
INT
PEND1, type R/W, offset 0x204, reset 0x0000.0000
INT
INT
UNPEND0, type R/W, offset 0x280, reset 0x0000.0000
INT
INT

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UNPEND1, type R/W, offset 0x284, reset 0x0000.0000															
									INT						
INT															
ACTIVE0, type RO, offset 0x300, reset 0x0000.0000															
INT															
INT															
ACTIVE1, type RO, offset 0x304, reset 0x0000.0000															
									INT						
INT															
PRI0, type R/W, offset 0x400, reset 0x0000.0000															
INTD								INTC							
INTB								INTA							
PRI1, type R/W, offset 0x404, reset 0x0000.0000															
INTD								INTC							
INTB								INTA							
PRI2, type R/W, offset 0x408, reset 0x0000.0000															
INTD								INTC							
INTB								INTA							
PRI3, type R/W, offset 0x40C, reset 0x0000.0000															
INTD								INTC							
INTB								INTA							
PRI4, type R/W, offset 0x410, reset 0x0000.0000															
INTD								INTC							
INTB								INTA							
PRI5, type R/W, offset 0x414, reset 0x0000.0000															
INTD								INTC							
INTB								INTA							
PRI6, type R/W, offset 0x418, reset 0x0000.0000															
INTD								INTC							
INTB								INTA							
PRI7, type R/W, offset 0x41C, reset 0x0000.0000															
INTD								INTC							
INTB								INTA							
PRI8, type R/W, offset 0x420, reset 0x0000.0000															
INTD								INTC							
INTB								INTA							
PRI9, type R/W, offset 0x424, reset 0x0000.0000															
INTD								INTC							
INTB								INTA							
PRI10, type R/W, offset 0x428, reset 0x0000.0000															
INTD								INTC							
INTB								INTA							
PRI11, type R/W, offset 0x42C, reset 0x0000.0000															
INTD								INTC							
INTB								INTA							
PRI12, type R/W, offset 0x430, reset 0x0000.0000															
INTD								INTC							
INTB								INTA							
PRI13, type R/W, offset 0x434, reset 0x0000.0000															
INTD								INTC							
INTB								INTA							

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SWTRIG, type WO, offset 0xF00, reset 0x0000.0000															
										INTID					
Cortex-M3 Peripherals **System Control Block (SCB) Registers** Base 0xE000.E000															
ACTLR, type R/W, offset 0x008, reset 0x0000.0000															
													DISFOLD	DISWBUF	DISMCYC
CPUID, type RO, offset 0xD00, reset 0x412F.C230															
IMP								VAR				CON			
PARTNO												REV			
INTCTRL, type R/W, offset 0xD04, reset 0x0000.0000															
NMISET			PENDSV	UNPENDSV	PENDSTSET	PENDSTCLR		ISRPRE	ISRPEND				VECPEND		
VECPEND				RETBASE					VECACT						
VTABLE, type R/W, offset 0xD08, reset 0x0000.0000															
		BASE	OFFSET												
OFFSET															
APINT, type R/W, offset 0xD0C, reset 0xFA05.0000															
VECTKEY															
ENDIANESS					PRIGROUP								SYSRESREQ	VECTCLRACT	VECTRESET
SYSCTRL, type R/W, offset 0xD10, reset 0x0000.0000															
											SEVONPEND		SLEEPDEEP	SLEEPEXIT	
CFGCTRL, type R/W, offset 0xD14, reset 0x0000.0200															
						STKALIGN	BFHFNMIGN				DIV0	UNALIGNED		MAINPEND	BASETHR
SYSPRI1, type R/W, offset 0xD18, reset 0x0000.0000															
								USAGE							
BUS								MEM							
SYSPRI2, type R/W, offset 0xD1C, reset 0x0000.0000															
SVC															
SYSPRI3, type R/W, offset 0xD20, reset 0x0000.0000															
TICK								PENDSV							
								DEBUG							
SYSHNDCTRL, type R/W, offset 0xD24, reset 0x0000.0000															
													USAGE	BUS	MEM
SVC	BUSP	MEMP	USAGEP	TICK	PNDSV		MON	SVCA				USGA		BUSA	MEMA
FAULTSTAT, type R/W1C, offset 0xD28, reset 0x0000.0000															
						DIV0	UNALIGN					NOCP	INVPC	INVSTAT	UNDEF
BFARV			BSTKE	BUSTKE	IMPRE	PRECISE	IBUS	MMARV			MSTKE	MUSTKE		DERR	IERR
HFAULTSTAT, type R/W1C, offset 0xD2C, reset 0x0000.0000															
DBG	FORCED														
														VECT	
MMADDR, type R/W, offset 0xD34, reset -															
ADDR															
ADDR															
FAULTADDR, type R/W, offset 0xD38, reset -															
ADDR															
ADDR															

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Cortex-M3 Peripherals **Memory Protection Unit (MPU) Registers** Base 0xE000.E000															
MPUTYPE, type RO, offset 0xD90, reset 0x0000.0800															
								IREGION							
DREGION															SEPARATE
MPUCTRL, type R/W, offset 0xD94, reset 0x0000.0000															
													PRIVDEFEN	HFNMIENA	ENABLE
MPUNUMBER, type R/W, offset 0xD98, reset 0x0000.0000															
													NUMBER		
MPUBASE, type R/W, offset 0xD9C, reset 0x0000.0000															
ADDR															
ADDR											VALID		REGION		
MPUBASE1, type R/W, offset 0xDA4, reset 0x0000.0000															
ADDR															
ADDR											VALID		REGION		
MPUBASE2, type R/W, offset 0xDAC, reset 0x0000.0000															
ADDR															
ADDR											VALID		REGION		
MPUBASE3, type R/W, offset 0xDB4, reset 0x0000.0000															
ADDR															
ADDR											VALID		REGION		
MPUATTR, type R/W, offset 0xDA0, reset 0x0000.0000															
			XN		AP					TEX			S	C	B
SRD										SIZE					ENABLE
MPUATTR1, type R/W, offset 0xDA8, reset 0x0000.0000															
			XN		AP					TEX			S	C	B
SRD										SIZE					ENABLE
MPUATTR2, type R/W, offset 0xDB0, reset 0x0000.0000															
			XN		AP					TEX			S	C	B
SRD										SIZE					ENABLE
MPUATTR3, type R/W, offset 0xDB8, reset 0x0000.0000															
			XN		AP					TEX			S	C	B
SRD										SIZE					ENABLE
System Control Base 0x400F.E000															
DID0, type RO, offset 0x000, reset - (see page 217)															
	VER							CLASS							
MAJOR								MINOR							
PBORCTL, type R/W, offset 0x030, reset 0x0000.7FFD (see page 219)															
														BORIOR	
RIS, type RO, offset 0x050, reset 0x0000.0000 (see page 220)															
							MOSCPUPRIS	USBPLLLRIS	PLLLRIS					BORRIS	
IMC, type R/W, offset 0x054, reset 0x0000.0000 (see page 222)															
							MOSCPUPIM	USBPLLLIM	PLLLIM					BORIM	

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISC, type R/W1C, offset 0x058, reset 0x0000.0000 (see page 224)															
							MOSCPUPMIS	USBPLLLMIS	PLLLMIS					BORMIS	
RESC, type R/W, offset 0x05C, reset - (see page 226)															
															MOSCFAIL
										WDT1	SW	WDT0	BOR	POR	EXT
RCC, type R/W, offset 0x060, reset 0x078E.3AD1 (see page 228)															
				ACG	SYSDIV				USESYSDIV		USEPWMDIV	PWMDIV			
		PWRDN		BYPASS	XTAL					OSCSRC				IOSCDIS	MOSCDIS
PLLCFG, type RO, offset 0x064, reset - (see page 233)															
		F									R				
GPIOHBCTL, type R/W, offset 0x06C, reset 0x0000.0000 (see page 234)															
							PORTJ	PORTH	PORTG	PORTF	PORTE	PORTD	PORTC	PORTB	PORTA
RCC2, type R/W, offset 0x070, reset 0x07C0.6810 (see page 236)															
USERCC2	DIV400		SYSDIV2						SYSDIV2LSB						
	USBPWRDN	PWRDN2		BYPASS2					OSCSRC2						
MOSCCTL, type R/W, offset 0x07C, reset 0x0000.0000 (see page 239)															
															CVAL
DSLPCLKCFG, type R/W, offset 0x144, reset 0x0780.0000 (see page 240)															
			DSDIVORIDE												
									DSOSCSRC						
PIOSCCAL, type R/W, offset 0x150, reset 0x0000.0000 (see page 242)															
UTEN															
							UPDATE		UT						
I2SMCLKCFG, type R/W, offset 0x170, reset 0x0000.0000 (see page 243)															
RXEN		RXI										RXF			
TXEN		TXI										TXF			
DID1, type RO, offset 0x004, reset - (see page 245)															
VER				FAM				PARTNO							
PINCOUNT								TEMP			PKG		ROHS	QUAL	
DC0, type RO, offset 0x008, reset 0x017F.007F (see page 247)															
SRAMSZ															
FLASHSZ															
DC1, type RO, offset 0x010, reset - (see page 248)															
			WDT1			CAN1	CAN0				PWM			ADC1	ADC0
MINSYSDIV				MAXADC1SPD		MAXADC0SPD		MPU		TEMPSNS	PLL	WDT0	SWO	SWD	JTAG
DC2, type RO, offset 0x014, reset 0x570F.5337 (see page 251)															
	EPI0		I2S0		COMP2	COMP1	COMP0					TIMER3	TIMER2	TIMER1	TIMER0
	I2C1		I2C0			QEI1	QEI0			SSI1	SSI0		UART2	UART1	UART0
DC3, type RO, offset 0x018, reset 0xBFFF.FFFF (see page 253)															
32KHZ		CCP5	CCP4	CCP3	CCP2	CCP1	CCP0	ADC0AIN7	ADC0AIN6	ADC0AIN5	ADC0AIN4	ADC0AIN3	ADC0AIN2	ADC0AIN1	ADC0AIN0
PWMFAULT	C2O	C2PLUS	C2MINUS	C1O	C1PLUS	C1MINUS	C0O	C0PLUS	C0MINUS	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0
DC4, type RO, offset 0x01C, reset 0x5104.F1FF (see page 256)															
	EPHY0		EMAC0				E1588						PICAL		
CCP7	CCP6	UDMA	ROM				GPIOJ	GPIOH	GPIOG	GPIOF	GPIOE	GPIOD	GPIOC	GPIOB	GPIOA
DC5, type RO, offset 0x020, reset 0x0F30.00FF (see page 258)															
				PWMFAULT3	PWMFAULT2	PWMFAULT1	PWMFAULT0			PWMEFLT	PWMESYNC				
								PWM7	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DC6, type RO, offset 0x024, reset 0x0000.0013 (see page 260)															
											USB0PHY			USB0	
DC7, type RO, offset 0x028, reset 0xFFFF.FFFF (see page 261)															
	DMACH30	DMACH29	DMACH28	DMACH27	DMACH26	DMACH25	DMACH24	DMACH23	DMACH22	DMACH21	DMACH20	DMACH19	DMACH18	DMACH17	DMACH16
DMACH15	DMACH14	DMACH13	DMACH12	DMACH11	DMACH10	DMACH9	DMACH8	DMACH7	DMACH6	DMACH5	DMACH4	DMACH3	DMACH2	DMACH1	DMACH0
DC8, type RO, offset 0x02C, reset 0xFFFF.FFFF (see page 265)															
ADC1AIN15	ADC1AIN14	ADC1AIN13	ADC1AIN12	ADC1AIN11	ADC1AIN10	ADC1AIN9	ADC1AIN8	ADC1AIN7	ADC1AIN6	ADC1AIN5	ADC1AIN4	ADC1AIN3	ADC1AIN2	ADC1AIN1	ADC1AIN0
ADC0AIN15	ADC0AIN14	ADC0AIN13	ADC0AIN12	ADC0AIN11	ADC0AIN10	ADC0AIN9	ADC0AIN8	ADC0AIN7	ADC0AIN6	ADC0AIN5	ADC0AIN4	ADC0AIN3	ADC0AIN2	ADC0AIN1	ADC0AIN0
DC9, type RO, offset 0x190, reset 0x00FF.00FF (see page 268)															
								ADC1DC7	ADC1DC6	ADC1DC5	ADC1DC4	ADC1DC3	ADC1DC2	ADC1DC1	ADC1DC0
								ADC0DC7	ADC0DC6	ADC0DC5	ADC0DC4	ADC0DC3	ADC0DC2	ADC0DC1	ADC0DC0
NVMSTAT, type RO, offset 0x1A0, reset 0x0000.0001 (see page 270)															
															FWB
RCGC0, type R/W, offset 0x100, reset 0x00000040 (see page 271)															
			WDT1			CAN1	CAN0				PWM			ADC1	ADC0
				MAXADC1SPD		MAXADC0SPD						WDT0			
SCGC0, type R/W, offset 0x110, reset 0x00000040 (see page 274)															
			WDT1			CAN1	CAN0				PWM			ADC1	ADC0
				MAXADC1SPD		MAXADC0SPD						WDT0			
DCGC0, type R/W, offset 0x120, reset 0x00000040 (see page 277)															
			WDT1			CAN1	CAN0				PWM			ADC1	ADC0
												WDT0			
RCGC1, type R/W, offset 0x104, reset 0x00000000 (see page 279)															
	EPI0		I2S0		COMP2	COMP1	COMP0					TIMER3	TIMER2	TIMER1	TIMER0
	I2C1		I2C0			QEI1	QEI0			SSI1	SSI0		UART2	UART1	UART0
SCGC1, type R/W, offset 0x114, reset 0x00000000 (see page 283)															
	EPI0		I2S0		COMP2	COMP1	COMP0					TIMER3	TIMER2	TIMER1	TIMER0
	I2C1		I2C0			QEI1	QEI0			SSI1	SSI0		UART2	UART1	UART0
DCGC1, type R/W, offset 0x124, reset 0x00000000 (see page 287)															
	EPI0		I2S0		COMP2	COMP1	COMP0					TIMER3	TIMER2	TIMER1	TIMER0
	I2C1		I2C0			QEI1	QEI0			SSI1	SSI0		UART2	UART1	UART0
RCGC2, type R/W, offset 0x108, reset 0x00000000 (see page 291)															
	EPHY0		EMAC0												USB0
		UDMA					GPIOJ	GPIOH	GPIOG	GPIOF	GPIOE	GPIOD	GPIOC	GPIOB	GPIOA
SCGC2, type R/W, offset 0x118, reset 0x00000000 (see page 294)															
	EPHY0		EMAC0												USB0
		UDMA					GPIOJ	GPIOH	GPIOG	GPIOF	GPIOE	GPIOD	GPIOC	GPIOB	GPIOA
DCGC2, type R/W, offset 0x128, reset 0x00000000 (see page 297)															
	EPHY0		EMAC0												USB0
		UDMA					GPIOJ	GPIOH	GPIOG	GPIOF	GPIOE	GPIOD	GPIOC	GPIOB	GPIOA
SRCR0, type R/W, offset 0x040, reset 0x00000000 (see page 300)															
			WDT1			CAN1	CAN0				PWM			ADC1	ADC0
												WDT0			
SRCR1, type R/W, offset 0x044, reset 0x00000000 (see page 302)															
	EPI0		I2S0		COMP2	COMP1	COMP0					TIMER3	TIMER2	TIMER1	TIMER0
	I2C1		I2C0			QEI1	QEI0			SSI1	SSI0		UART2	UART1	UART0
SRCR2, type R/W, offset 0x048, reset 0x00000000 (see page 305)															
	EPHY0		EMAC0												USB0
		UDMA					GPIOJ	GPIOH	GPIOG	GPIOF	GPIOE	GPIOD	GPIOC	GPIOB	GPIOA

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Internal Memory **Flash Memory Registers (Flash Control Offset)** Base 0x400F.D000															
FMA, type R/W, offset 0x000, reset 0x0000.0000															
														OFFSET	
OFFSET															
FMD, type R/W, offset 0x004, reset 0x0000.0000															
DATA															
DATA															
FMC, type R/W, offset 0x008, reset 0x0000.0000															
WRKEY															
												COMT	MERASE	ERASE	WRITE
FCRIS, type RO, offset 0x00C, reset 0x0000.0000															
														PRIS	ARIS
FCIM, type R/W, offset 0x010, reset 0x0000.0000															
														PMASK	AMASK
FCMISC, type R/W1C, offset 0x014, reset 0x0000.0000															
														PMISC	AMISC
FMC2, type R/W, offset 0x020, reset 0x0000.0000															
WRKEY															
															WRBUF
FWBVAL, type R/W, offset 0x030, reset 0x0000.0000															
FWB[n]															
FWB[n]															
FCTL, type R/W, offset 0x0F8, reset 0x0000.0000															
														USDACK	USDREQ
FWBn, type R/W, offset 0x100 - 0x17C, reset 0x0000.0000															
DATA															
DATA															
Internal Memory **Memory Registers (System Control Offset)** Base 0x400F.E000															
RMCTL, type R/W1C, offset 0x0F0, reset -															
															BA
FMPRE0, type R/W, offset 0x130 and 0x200, reset 0xFFFF.FFFF															
READ_ENABLE															
READ_ENABLE															
FMPPE0, type R/W, offset 0x134 and 0x400, reset 0xFFFF.FFFF															
PROG_ENABLE															
PROG_ENABLE															
BOOTCFG, type R/W, offset 0x1D0, reset 0xFFFF.FFFE															
NW															
PORT				PIN			POL	EN						DBG1	DBG0
USER_REG0, type R/W, offset 0x1E0, reset 0xFFFF.FFFF															
NW	DATA														
DATA															

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USER_REG1, type R/W, offset 0x1E4, reset 0xFFFF.FFFF															
NW	DATA														
DATA															
USER_REG2, type R/W, offset 0x1E8, reset 0xFFFF.FFFF															
NW	DATA														
DATA															
USER_REG3, type R/W, offset 0x1EC, reset 0xFFFF.FFFF															
NW	DATA														
DATA															
FMPRE1, type R/W, offset 0x204, reset 0xFFFF.FFFF															
READ_ENABLE															
READ_ENABLE															
FMPRE2, type R/W, offset 0x208, reset 0xFFFF.FFFF															
READ_ENABLE															
READ_ENABLE															
FMPRE3, type R/W, offset 0x20C, reset 0xFFFF.FFFF															
READ_ENABLE															
READ_ENABLE															
FMPPE1, type R/W, offset 0x404, reset 0xFFFF.FFFF															
PROG_ENABLE															
PROG_ENABLE															
FMPPE2, type R/W, offset 0x408, reset 0xFFFF.FFFF															
PROG_ENABLE															
PROG_ENABLE															
FMPPE3, type R/W, offset 0x40C, reset 0xFFFF.FFFF															
PROG_ENABLE															
PROG_ENABLE															
Micro Direct Memory Access (µDMA) **µDMA Channel Control Structure (Offset from Channel Control Table Base)** Base n/a															
DMASRCENDP, type R/W, offset 0x000, reset -															
ADDR															
ADDR															
DMADSTENDP, type R/W, offset 0x004, reset -															
ADDR															
ADDR															
DMACHCTL, type R/W, offset 0x008, reset -															
DSTINC	DSTSIZE			SRCINC		SRCSIZE								ARBSIZE	
ARBSIZE	XFERSIZE											NXTUSEBURST	XFERMODE		
Micro Direct Memory Access (µDMA) **µDMA Registers (Offset from µDMA Base Address)** Base 0x400F.F000															
DMASTAT, type RO, offset 0x000, reset 0x001F.0000															
											DMACHANS				
								STATE							MASTEN
DMACFG, type WO, offset 0x004, reset -															
															MASTEN
DMACTLBASE, type R/W, offset 0x008, reset 0x0000.0000															
ADDR															
ADDR															

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMAALTBASE, type RO, offset 0x00C, reset 0x0000.0200															
ADDR															
ADDR															
DMAWAITSTAT, type RO, offset 0x010, reset 0xFFFF.FFC0															
WAITREQ[n]															
WAITREQ[n]															
DMASWREQ, type WO, offset 0x014, reset -															
SWREQ[n]															
SWREQ[n]															
DMAUSEBURSTSET, type R/W, offset 0x018, reset 0x0000.0000															
SET[n]															
SET[n]															
DMAUSEBURSTCLR, type WO, offset 0x01C, reset -															
CLR[n]															
CLR[n]															
DMAREQMASKSET, type R/W, offset 0x020, reset 0x0000.0000															
SET[n]															
SET[n]															
DMAREQMASKCLR, type WO, offset 0x024, reset -															
CLR[n]															
CLR[n]															
DMAENASET, type R/W, offset 0x028, reset 0x0000.0000															
SET[n]															
SET[n]															
DMAENACLR, type WO, offset 0x02C, reset -															
CLR[n]															
CLR[n]															
DMAALTSET, type R/W, offset 0x030, reset 0x0000.0000															
SET[n]															
SET[n]															
DMAALTCLR, type WO, offset 0x034, reset -															
CLR[n]															
CLR[n]															
DMAPRIOSET, type R/W, offset 0x038, reset 0x0000.0000															
SET[n]															
SET[n]															
DMAPRIOCLR, type WO, offset 0x03C, reset -															
CLR[n]															
CLR[n]															
DMAERRCLR, type R/W, offset 0x04C, reset 0x0000.0000															
															ERRCLR
DMACHASGN, type R/W, offset 0x500, reset 0x0000.0000															
CHASGN[n]															
CHASGN[n]															
DMAPeriphID0, type RO, offset 0xFE0, reset 0x0000.0030															
								PID0							
DMAPeriphID1, type RO, offset 0xFE4, reset 0x0000.00B2															
								PID1							

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMAPeriphID2, type RO, offset 0xFE8, reset 0x0000.000B															
								PID2							
DMAPeriphID3, type RO, offset 0xFEC, reset 0x0000.0000															
								PID3							
DMAPeriphID4, type RO, offset 0xFD0, reset 0x0000.0004															
								PID4							
DMAPCellID0, type RO, offset 0xFF0, reset 0x0000.000D															
								CID0							
DMAPCellID1, type RO, offset 0xFF4, reset 0x0000.00F0															
								CID1							
DMAPCellID2, type RO, offset 0xFF8, reset 0x0000.0005															
								CID2							
DMAPCellID3, type RO, offset 0xFFC, reset 0x0000.00B1															
								CID3							

General-Purpose Input/Outputs (GPIOs)

GPIO Port A (APB) base: 0x4000.4000
GPIO Port A (AHB) base: 0x4005.8000
GPIO Port B (APB) base: 0x4000.5000
GPIO Port B (AHB) base: 0x4005.9000
GPIO Port C (APB) base: 0x4000.6000
GPIO Port C (AHB) base: 0x4005.A000
GPIO Port D (APB) base: 0x4000.7000
GPIO Port D (AHB) base: 0x4005.B000
GPIO Port E (APB) base: 0x4002.4000
GPIO Port E (AHB) base: 0x4005.C000
GPIO Port F (APB) base: 0x4002.5000
GPIO Port F (AHB) base: 0x4005.D000
GPIO Port G (APB) base: 0x4002.6000
GPIO Port G (AHB) base: 0x4005.E000
GPIO Port H (APB) base: 0x4002.7000
GPIO Port H (AHB) base: 0x4005.F000
GPIO Port J (APB) base: 0x4003.D000
GPIO Port J (AHB) base: 0x4006.0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIODATA, type R/W, offset 0x000, reset 0x0000.0000 (see page 416)															
								DATA							
GPIODIR, type R/W, offset 0x400, reset 0x0000.0000 (see page 417)															
								DIR							
GPIOIS, type R/W, offset 0x404, reset 0x0000.0000 (see page 418)															
								IS							
GPIOIBE, type R/W, offset 0x408, reset 0x0000.0000 (see page 419)															
								IBE							
GPIOIEV, type R/W, offset 0x40C, reset 0x0000.0000 (see page 420)															
								IEV							
GPIOIM, type R/W, offset 0x410, reset 0x0000.0000 (see page 421)															
								IME							

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIORIS, type RO, offset 0x414, reset 0x0000.0000 (see page 422)															
								RIS							
GPIOMIS, type RO, offset 0x418, reset 0x0000.0000 (see page 423)															
								MIS							
GPIOICR, type W1C, offset 0x41C, reset 0x0000.0000 (see page 425)															
								IC							
GPIOAFSEL, type R/W, offset 0x420, reset - (see page 426)															
								AFSEL							
GPIODR2R, type R/W, offset 0x500, reset 0x0000.00FF (see page 428)															
								DRV2							
GPIODR4R, type R/W, offset 0x504, reset 0x0000.0000 (see page 429)															
								DRV4							
GPIODR8R, type R/W, offset 0x508, reset 0x0000.0000 (see page 430)															
								DRV8							
GPIOODR, type R/W, offset 0x50C, reset 0x0000.0000 (see page 431)															
								ODE							
GPIOPUR, type R/W, offset 0x510, reset - (see page 432)															
								PUE							
GPIOPDR, type R/W, offset 0x514, reset 0x0000.0000 (see page 434)															
								PDE							
GPIOSLR, type R/W, offset 0x518, reset 0x0000.0000 (see page 436)															
								SRL							
GPIODEN, type R/W, offset 0x51C, reset - (see page 437)															
								DEN							
GPIOLOCK, type R/W, offset 0x520, reset 0x0000.0001 (see page 439)															
								LOCK							
								LOCK							
GPIOCR, type -, offset 0x524, reset - (see page 440)															
								CR							
GPIOAMSEL, type R/W, offset 0x528, reset 0x0000.0000 (see page 442)															
								GPIOAMSEL							
GPIOPCTL, type R/W, offset 0x52C, reset - (see page 444)															
PMC7				PMC6				PMC5				PMC4			
PMC3				PMC2				PMC1				PMC0			
GPIOPeriphID4, type RO, offset 0xFD0, reset 0x0000.0000 (see page 446)															
								PID4							

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIOPeriphID5, type RO, offset 0xFD4, reset 0x0000.0000 (see page 447)															
								PID5							
GPIOPeriphID6, type RO, offset 0xFD8, reset 0x0000.0000 (see page 448)															
								PID6							
GPIOPeriphID7, type RO, offset 0xFDC, reset 0x0000.0000 (see page 449)															
								PID7							
GPIOPeriphID0, type RO, offset 0xFE0, reset 0x0000.0061 (see page 450)															
								PID0							
GPIOPeriphID1, type RO, offset 0xFE4, reset 0x0000.0000 (see page 451)															
								PID1							
GPIOPeriphID2, type RO, offset 0xFE8, reset 0x0000.0018 (see page 452)															
								PID2							
GPIOPeriphID3, type RO, offset 0xFEC, reset 0x0000.0001 (see page 453)															
								PID3							
GPIOPCellID0, type RO, offset 0xFF0, reset 0x0000.000D (see page 454)															
								CID0							
GPIOPCellID1, type RO, offset 0xFF4, reset 0x0000.00F0 (see page 455)															
								CID1							
GPIOPCellID2, type RO, offset 0xFF8, reset 0x0000.0005 (see page 456)															
								CID2							
GPIOPCellID3, type RO, offset 0xFFC, reset 0x0000.00B1 (see page 457)															
								CID3							
External Peripheral Interface (EPI) Base 0x400D.0000															
EPICFG, type R/W, offset 0x000, reset 0x0000.0000 (see page 490)															
											BLKEN	MODE			
EPIBAUD, type R/W, offset 0x004, reset 0x0000.0000 (see page 491)															
COUNT1															
COUNT0															
EPISDRAMCFG, type R/W, offset 0x010, reset 0x82EE.0000 (see page 493)															
FREQ					RFSH										
						SLEEP								SIZE	
EPIHB8CFG, type R/W, offset 0x010, reset 0x0000.FF00 (see page 495)															
								XFFEN	XFEEN	WRHIGH	RDHIGH				
MAXWAIT								WRWS		RDWS				MODE	
EPIHB16CFG, type R/W, offset 0x010, reset 0x0000.FF00 (see page 498)															
								XFFEN	XFEEN	WRHIGH	RDHIGH				
MAXWAIT								WRWS		RDWS			BSEL	MODE	
EPIGPCFG, type R/W, offset 0x010, reset 0x0000.0000 (see page 502)															
CLKPIN	CLKGATE		RDYEN	FRMPIN	FRM50	FRMCNT				RW		WR2CYC	RD2CYC		
MAXWAIT										ASIZE				DSIZE	

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EPIHB8CFG2, type R/W, offset 0x014, reset 0x0000.0000 (see page 507)															
WORD					CSBAUD	CSCFG									
EPIHB16CFG2, type R/W, offset 0x014, reset 0x0000.0000 (see page 509)															
WORD					CSBAUD	CSCFG									
EPIGPCFG2, type R/W, offset 0x014, reset 0x0000.0000 (see page 511)															
WORD															
EPIADDRMAP, type R/W, offset 0x01C, reset 0x0000.0000 (see page 512)															
								EPSZ		EPADR		ERSZ		ERADR	
EPIRSIZE0, type R/W, offset 0x020, reset 0x0000.0003 (see page 514)															
														SIZE	
EPIRSIZE1, type R/W, offset 0x030, reset 0x0000.0003 (see page 514)															
														SIZE	
EPIRADDR0, type R/W, offset 0x024, reset 0x0000.0000 (see page 515)															
			ADDR												
ADDR															
EPIRADDR1, type R/W, offset 0x034, reset 0x0000.0000 (see page 515)															
			ADDR												
ADDR															
EPIRPSTD0, type R/W, offset 0x028, reset 0x0000.0000 (see page 516)															
			POSTCNT												
EPIRPSTD1, type R/W, offset 0x038, reset 0x0000.0000 (see page 516)															
			POSTCNT												
EPISTAT, type RO, offset 0x060, reset 0x0000.0000 (see page 518)															
						CELOW	XFFULL	XFEMPTY	INITSEQ	WBUSY	NBRBUSY				ACTIVE
EPIRFIFOCNT, type RO, offset 0x06C, reset - (see page 520)															
												COUNT			
EPIREADFIFO, type RO, offset 0x070, reset - (see page 521)															
DATA															
DATA															
EPIREADFIFO1, type RO, offset 0x074, reset - (see page 521)															
DATA															
DATA															
EPIREADFIFO2, type RO, offset 0x078, reset - (see page 521)															
DATA															
DATA															
EPIREADFIFO3, type RO, offset 0x07C, reset - (see page 521)															
DATA															
DATA															
EPIREADFIFO4, type RO, offset 0x080, reset - (see page 521)															
DATA															
DATA															

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EPIREADFIFO5, type RO, offset 0x084, reset - (see page 521)															
DATA															
DATA															
EPIREADFIFO6, type RO, offset 0x088, reset - (see page 521)															
DATA															
DATA															
EPIREADFIFO7, type RO, offset 0x08C, reset - (see page 521)															
DATA															
DATA															
EPIFIFOLVL, type R/W, offset 0x200, reset 0x0000.0033 (see page 522)															
														WFERR	RSERR
									WRFIFO				RDFIFO		
EPIWFIFOCNT, type RO, offset 0x204, reset 0x0000.0004 (see page 524)															
													WTAV		
EPIIM, type R/W, offset 0x210, reset 0x0000.0000 (see page 525)															
													WRIM	RDIM	ERRIM
EPIRIS, type RO, offset 0x214, reset 0x0000.0004 (see page 526)															
													WRRIS	RDRIS	ERRRIS
EPIMIS, type RO, offset 0x218, reset 0x0000.0000 (see page 528)															
													WRMIS	RDMIS	ERRMIS
EPIEISC, type R/W1C, offset 0x21C, reset 0x0000.0000 (see page 529)															
													WTFULL	RSTALL	TOUT
General-Purpose Timers Timer 0 base: 0x4003.0000 Timer 1 base: 0x4003.1000 Timer 2 base: 0x4003.2000 Timer 3 base: 0x4003.3000															
GPTMCFG, type R/W, offset 0x000, reset 0x0000.0000 (see page 548)															
													GPTMCFG		
GPTMTAMR, type R/W, offset 0x004, reset 0x0000.0000 (see page 549)															
								TASNAPS	TAWOT	TAMIE	TACDIR	TAAMS	TACMR	TAMR	
GPTMTBMR, type R/W, offset 0x008, reset 0x0000.0000 (see page 551)															
								TBSNAPS	TBWOT	TBMIE	TBCDIR	TBAMS	TBCMR	TBMR	
GPTMCTL, type R/W, offset 0x00C, reset 0x0000.0000 (see page 553)															
	TBPWML	TBOTE		TBEVENT		TBSTALL	TBEN		TAPWML	TAOTE	RTCEN	TAEVENT		TASTALL	TAEN
GPTMIMR, type R/W, offset 0x018, reset 0x0000.0000 (see page 556)															
				TBMIM	CBEIM	CBMIM	TBTOIM				TAMIM	RTCIM	CAEIM	CAMIM	TATOIM
GPTMRIS, type RO, offset 0x01C, reset 0x0000.0000 (see page 558)															
				TBMRIS	CBERIS	CBMRIS	TBTORIS				TAMRIS	RTCRIS	CAERIS	CAMRIS	TATORIS
GPTMMIS, type RO, offset 0x020, reset 0x0000.0000 (see page 561)															
				TBMMIS	CBEMIS	CBMMIS	TBTOMIS				TAMMIS	RTCMIS	CAEMIS	CAMMIS	TATOMIS

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPTMICR, type W1C, offset 0x024, reset 0x0000.0000 (see page 564)															
				TBMCINT	CBECINT	CBMCINT	TBTOCINT				TAMCINT	RTCCINT	CAECINT	CAMCINT	TATOCINT
GPTMTAILR, type R/W, offset 0x028, reset 0xFFFF.FFFF (see page 566)															
TAILR															
TAILR															
GPTMTBILR, type R/W, offset 0x02C, reset 0x0000.FFFF (see page 567)															
TBILR															
TBILR															
GPTMTAMATCHR, type R/W, offset 0x030, reset 0xFFFF.FFFF (see page 568)															
TAMR															
TAMR															
GPTMTBMATCHR, type R/W, offset 0x034, reset 0x0000.FFFF (see page 569)															
TBMR															
TBMR															
GPTMTAPR, type R/W, offset 0x038, reset 0x0000.0000 (see page 570)															
								TAPSR							
GPTMTBPR, type R/W, offset 0x03C, reset 0x0000.0000 (see page 571)															
								TBPSR							
GPTMTAPMR, type R/W, offset 0x040, reset 0x0000.0000 (see page 572)															
								TAPSMR							
GPTMTBPMR, type R/W, offset 0x044, reset 0x0000.0000 (see page 573)															
								TBPSMR							
GPTMTAR, type RO, offset 0x048, reset 0xFFFF.FFFF (see page 574)															
TAR															
TAR															
GPTMTBR, type RO, offset 0x04C, reset 0x0000.FFFF (see page 575)															
TBR															
TBR															
GPTMTAV, type RW, offset 0x050, reset 0xFFFF.FFFF (see page 576)															
TAV															
TAV															
GPTMTBV, type RW, offset 0x054, reset 0x0000.FFFF (see page 577)															
TBV															
TBV															
Watchdog Timers WDT0 base: 0x4000.0000 WDT1 base: 0x4000.1000															
WDTLOAD, type R/W, offset 0x000, reset 0xFFFF.FFFF (see page 582)															
WDTLOAD															
WDTLOAD															
WDTVALUE, type RO, offset 0x004, reset 0xFFFF.FFFF (see page 583)															
WDTVALUE															
WDTVALUE															
WDTCTL, type R/W, offset 0x008, reset 0x0000.0000 (WDT0) and 0x8000.0000 (WDT1) (see page 584)															
WRC															
														RESEN	INTEN

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WDTICR, type WO, offset 0x00C, reset - (see page 586)															
WDTINTCLR															
WDTINTCLR															
WDTRIS, type RO, offset 0x010, reset 0x0000.0000 (see page 587)															
															WDTRIS
WDTMIS, type RO, offset 0x014, reset 0x0000.0000 (see page 588)															
															WDTMIS
WDTTEST, type R/W, offset 0x418, reset 0x0000.0000 (see page 589)															
							STALL								
WDTLOCK, type R/W, offset 0xC00, reset 0x0000.0000 (see page 590)															
WDTLOCK															
WDTLOCK															
WDTPeriphID4, type RO, offset 0xFD0, reset 0x0000.0000 (see page 591)															
								PID4							
WDTPeriphID5, type RO, offset 0xFD4, reset 0x0000.0000 (see page 592)															
								PID5							
WDTPeriphID6, type RO, offset 0xFD8, reset 0x0000.0000 (see page 593)															
								PID6							
WDTPeriphID7, type RO, offset 0xFDC, reset 0x0000.0000 (see page 594)															
								PID7							
WDTPeriphID0, type RO, offset 0xFE0, reset 0x0000.0005 (see page 595)															
								PID0							
WDTPeriphID1, type RO, offset 0xFE4, reset 0x0000.0018 (see page 596)															
								PID1							
WDTPeriphID2, type RO, offset 0xFE8, reset 0x0000.0018 (see page 597)															
								PID2							
WDTPeriphID3, type RO, offset 0xFEC, reset 0x0000.0001 (see page 598)															
								PID3							
WDTPCellID0, type RO, offset 0xFF0, reset 0x0000.000D (see page 599)															
								CID0							
WDTPCellID1, type RO, offset 0xFF4, reset 0x0000.00F0 (see page 600)															
								CID1							
WDTPCellID2, type RO, offset 0xFF8, reset 0x0000.0006 (see page 601)															
								CID2							
WDTPCellID3, type RO, offset 0xFFC, reset 0x0000.00B1 (see page 602)															
								CID3							

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Analog-to-Digital Converter (ADC) ADC0 base: 0x4003.8000 ADC1 base: 0x4003.9000															
ADCACTSS, type R/W, offset 0x000, reset 0x0000.0000 (see page 626)															
												ASEN3	ASEN2	ASEN1	ASEN0
ADCRIS, type RO, offset 0x004, reset 0x0000.0000 (see page 627)															
															INRDC
												INR3	INR2	INR1	INR0
ADCIM, type R/W, offset 0x008, reset 0x0000.0000 (see page 629)															
												DCONSS3	DCONSS2	DCONSS1	DCONSS0
												MASK3	MASK2	MASK1	MASK0
ADCISC, type R/W1C, offset 0x00C, reset 0x0000.0000 (see page 631)															
												DCINSS3	DCINSS2	DCINSS1	DCINSS0
												IN3	IN2	IN1	IN0
ADCOSTAT, type R/W1C, offset 0x010, reset 0x0000.0000 (see page 634)															
												OV3	OV2	OV1	OV0
ADCEMUX, type R/W, offset 0x014, reset 0x0000.0000 (see page 636)															
EM3				EM2				EM1				EM0			
ADCUSTAT, type R/W1C, offset 0x018, reset 0x0000.0000 (see page 641)															
												UV3	UV2	UV1	UV0
ADCSSPRI, type R/W, offset 0x020, reset 0x0000.3210 (see page 642)															
		SS3				SS2				SS1				SS0	
ADCSPC, type R/W, offset 0x024, reset 0x0000.0000 (see page 644)															
												PHASE			
ADCPSSI, type R/W, offset 0x028, reset - (see page 646)															
GSYNC				SYNCWAIT											
												SS3	SS2	SS1	SS0
ADCSAC, type R/W, offset 0x030, reset 0x0000.0000 (see page 648)															
													AVG		
ADCDCISC, type R/W1C, offset 0x034, reset 0x0000.0000 (see page 649)															
								DCINT7	DCINT6	DCINT5	DCINT4	DCINT3	DCINT2	DCINT1	DCINT0
ADCCTL, type R/W, offset 0x038, reset 0x0000.0000 (see page 651)															
															VREF
ADCSSMUX0, type R/W, offset 0x040, reset 0x0000.0000 (see page 652)															
MUX7				MUX6				MUX5				MUX4			
MUX3				MUX2				MUX1				MUX0			
ADCSSCTL0, type R/W, offset 0x044, reset 0x0000.0000 (see page 654)															
TS7	IE7	END7	D7	TS6	IE6	END6	D6	TS5	IE5	END5	D5	TS4	IE4	END4	D4
TS3	IE3	END3	D3	TS2	IE2	END2	D2	TS1	IE1	END1	D1	TS0	IE0	END0	D0
ADCSSFIFO0, type RO, offset 0x048, reset - (see page 657)															
						DATA									

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADCSSFIFO1, type RO, offset 0x068, reset - (see page 657)															
						DATA									
ADCSSFIFO2, type RO, offset 0x088, reset - (see page 657)															
						DATA									
ADCSSFIFO3, type RO, offset 0x0A8, reset - (see page 657)															
						DATA									
ADCSSFSTAT0, type RO, offset 0x04C, reset 0x0000.0100 (see page 658)															
			FULL				EMPTY		HPTR				TPTR		
ADCSSFSTAT1, type RO, offset 0x06C, reset 0x0000.0100 (see page 658)															
			FULL				EMPTY		HPTR				TPTR		
ADCSSFSTAT2, type RO, offset 0x08C, reset 0x0000.0100 (see page 658)															
			FULL				EMPTY		HPTR				TPTR		
ADCSSFSTAT3, type RO, offset 0x0AC, reset 0x0000.0100 (see page 658)															
			FULL				EMPTY		HPTR				TPTR		
ADCSSOP0, type R/W, offset 0x050, reset 0x0000.0000 (see page 660)															
			S7DCOP				S6DCOP				S5DCOP				S4DCOP
			S3DCOP				S2DCOP				S1DCOP				S0DCOP
ADCSSDC0, type R/W, offset 0x054, reset 0x0000.0000 (see page 662)															
S7DCSEL				S6DCSEL				S5DCSEL				S4DCSEL			
S3DCSEL				S2DCSEL				S1DCSEL				S0DCSEL			
ADCSSMUX1, type R/W, offset 0x060, reset 0x0000.0000 (see page 664)															
MUX3				MUX2				MUX1				MUX0			
ADCSSMUX2, type R/W, offset 0x080, reset 0x0000.0000 (see page 664)															
MUX3				MUX2				MUX1				MUX0			
ADCSSCTL1, type R/W, offset 0x064, reset 0x0000.0000 (see page 665)															
TS3	IE3	END3	D3	TS2	IE2	END2	D2	TS1	IE1	END1	D1	TS0	IE0	END0	D0
ADCSSCTL2, type R/W, offset 0x084, reset 0x0000.0000 (see page 665)															
TS3	IE3	END3	D3	TS2	IE2	END2	D2	TS1	IE1	END1	D1	TS0	IE0	END0	D0
ADCSSOP1, type R/W, offset 0x070, reset 0x0000.0000 (see page 667)															
			S3DCOP				S2DCOP				S1DCOP				S0DCOP
ADCSSOP2, type R/W, offset 0x090, reset 0x0000.0000 (see page 667)															
			S3DCOP				S2DCOP				S1DCOP				S0DCOP
ADCSSDC1, type R/W, offset 0x074, reset 0x0000.0000 (see page 668)															
S3DCSEL				S2DCSEL				S1DCSEL				S0DCSEL			
ADCSSDC2, type R/W, offset 0x094, reset 0x0000.0000 (see page 668)															
S3DCSEL				S2DCSEL				S1DCSEL				S0DCSEL			

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADCSSMUX3, type R/W, offset 0x0A0, reset 0x0000.0000 (see page 670)															
												MUX0			
ADCSSCTL3, type R/W, offset 0x0A4, reset 0x0000.0002 (see page 671)															
												TS0	IE0	END0	D0
ADCSSOP3, type R/W, offset 0x0B0, reset 0x0000.0000 (see page 672)															
															S0DCOP
ADCSSDC3, type R/W, offset 0x0B4, reset 0x0000.0000 (see page 673)															
												S0DCSEL			
ADCDCRIC, type R/W, offset 0xD00, reset 0x0000.0000 (see page 674)															
								DCTRIG7	DCTRIG6	DCTRIG5	DCTRIG4	DCTRIG3	DCTRIG2	DCTRIG1	DCTRIG0
								DCINT7	DCINT6	DCINT5	DCINT4	DCINT3	DCINT2	DCINT1	DCINT0
ADCDCCTL0, type R/W, offset 0xE00, reset 0x0000.0000 (see page 679)															
			CTE	CTC		CTM					CIE	CIC		CIM	
ADCDCCTL1, type R/W, offset 0xE04, reset 0x0000.0000 (see page 679)															
			CTE	CTC		CTM					CIE	CIC		CIM	
ADCDCCTL2, type R/W, offset 0xE08, reset 0x0000.0000 (see page 679)															
			CTE	CTC		CTM					CIE	CIC		CIM	
ADCDCCTL3, type R/W, offset 0xE0C, reset 0x0000.0000 (see page 679)															
			CTE	CTC		CTM					CIE	CIC		CIM	
ADCDCCTL4, type R/W, offset 0xE10, reset 0x0000.0000 (see page 679)															
			CTE	CTC		CTM					CIE	CIC		CIM	
ADCDCCTL5, type R/W, offset 0xE14, reset 0x0000.0000 (see page 679)															
			CTE	CTC		CTM					CIE	CIC		CIM	
ADCDCCTL6, type R/W, offset 0xE18, reset 0x0000.0000 (see page 679)															
			CTE	CTC		CTM					CIE	CIC		CIM	
ADCDCCTL7, type R/W, offset 0xE1C, reset 0x0000.0000 (see page 679)															
			CTE	CTC		CTM					CIE	CIC		CIM	
ADCDCCMP0, type R/W, offset 0xE40, reset 0x0000.0000 (see page 682)															
										COMP1					
										COMP0					
ADCDCCMP1, type R/W, offset 0xE44, reset 0x0000.0000 (see page 682)															
										COMP1					
										COMP0					
ADCDCCMP2, type R/W, offset 0xE48, reset 0x0000.0000 (see page 682)															
										COMP1					
										COMP0					
ADCDCCMP3, type R/W, offset 0xE4C, reset 0x0000.0000 (see page 682)															
										COMP1					
										COMP0					

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADCDCCMP4, type R/W, offset 0xE50, reset 0x0000.0000 (see page 682)															
						COMP1									
						COMP0									
ADCDCCMP5, type R/W, offset 0xE54, reset 0x0000.0000 (see page 682)															
						COMP1									
						COMP0									
ADCDCCMP6, type R/W, offset 0xE58, reset 0x0000.0000 (see page 682)															
						COMP1									
						COMP0									
ADCDCCMP7, type R/W, offset 0xE5C, reset 0x0000.0000 (see page 682)															
						COMP1									
						COMP0									
Universal Asynchronous Receivers/Transmitters (UARTs) UART0 base: 0x4000.C000 UART1 base: 0x4000.D000 UART2 base: 0x4000.E000															
UARTDR, type R/W, offset 0x000, reset 0x0000.0000 (see page 698)															
				OE	BE	PE	FE	DATA							
UARTRSR/UARTECR, type RO, offset 0x004, reset 0x0000.0000 (Read-Only Status Register) (see page 700)															
												OE	BE	PE	FE
UARTRSR/UARTECR, type WO, offset 0x004, reset 0x0000.0000 (Write-Only Error Clear Register) (see page 700)															
								DATA							
UARTFR, type RO, offset 0x018, reset 0x0000.0090 (see page 703)															
							RI	TXFE	RXFF	TXFF	RXFE	BUSY	DCD	DSR	CTS
UARTILPR, type R/W, offset 0x020, reset 0x0000.0000 (see page 706)															
								ILPDVSR							
UARTIBRD, type R/W, offset 0x024, reset 0x0000.0000 (see page 707)															
							DIVINT								
UARTFBRD, type R/W, offset 0x028, reset 0x0000.0000 (see page 708)															
										DIVFRAC					
UARTLCRH, type R/W, offset 0x02C, reset 0x0000.0000 (see page 709)															
								SPS	WLEN		FEN	STP2	EPS	PEN	BRK
UARTCTL, type R/W, offset 0x030, reset 0x0000.0300 (see page 711)															
CTSEN	RTSEN			RTS	DTR	RXE	TXE	LBE	LIN	HSE	EOT	SMART	SIRLP	SIREN	UARTEN
UARTIFLS, type R/W, offset 0x034, reset 0x0000.0012 (see page 715)															
										RXIFLSEL			TXIFLSEL		
UARTIM, type R/W, offset 0x038, reset 0x0000.0000 (see page 717)															
LME5IM	LME1IM	LMSBIM			OEIM	BEIM	PEIM	FEIM	RTIM	TXIM	RXIM	DSRIM	DCDIM	CTSIM	RIIM
UARTRIS, type RO, offset 0x03C, reset 0x0000.000F (see page 721)															
LME5RIS	LME1RIS	LMSBRIS			OERIS	BERIS	PERIS	FERIS	RTRIS	TXRIS	RXRIS	DSRRIS	DCDRIS	CTSRIS	RIRIS

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UARTMIS, type RO, offset 0x040, reset 0x0000.0000 (see page 725)															
LME5MIS	LME1MIS	LMSBMIS			OEMIS	BEMIS	PEMIS	FEMIS	RTMIS	TXMIS	RXMIS	DSRMIS	DCDMIS	CTSMIS	RIMIS
UARTICR, type W1C, offset 0x044, reset 0x0000.0000 (see page 729)															
LME5IC	LME1IC	LMSBIC			OEIC	BEIC	PEIC	FEIC	RTIC	TXIC	RXIC	DSRMIC	DCDMIC	CTSMIC	RIMIC
UARTDMACTL, type R/W, offset 0x048, reset 0x0000.0000 (see page 731)															
													DMAERR	TXDMAE	RXDMAE
UARTLCTL, type R/W, offset 0x090, reset 0x0000.0000 (see page 732)															
										BLEN					MASTER
UARTLSS, type RO, offset 0x094, reset 0x0000.0000 (see page 733)															
TSS															
UARTLTIM, type RO, offset 0x098, reset 0x0000.0000 (see page 734)															
TIMER															
UARTPeriphID4, type RO, offset 0xFD0, reset 0x0000.0000 (see page 735)															
								PID4							
UARTPeriphID5, type RO, offset 0xFD4, reset 0x0000.0000 (see page 736)															
								PID5							
UARTPeriphID6, type RO, offset 0xFD8, reset 0x0000.0000 (see page 737)															
								PID6							
UARTPeriphID7, type RO, offset 0xFDC, reset 0x0000.0000 (see page 738)															
								PID7							
UARTPeriphID0, type RO, offset 0xFE0, reset 0x0000.0060 (see page 739)															
								PID0							
UARTPeriphID1, type RO, offset 0xFE4, reset 0x0000.0000 (see page 740)															
								PID1							
UARTPeriphID2, type RO, offset 0xFE8, reset 0x0000.0018 (see page 741)															
								PID2							
UARTPeriphID3, type RO, offset 0xFEC, reset 0x0000.0001 (see page 742)															
								PID3							
UARTPCellID0, type RO, offset 0xFF0, reset 0x0000.000D (see page 743)															
								CID0							
UARTPCellID1, type RO, offset 0xFF4, reset 0x0000.00F0 (see page 744)															
								CID1							
UARTPCellID2, type RO, offset 0xFF8, reset 0x0000.0005 (see page 745)															
								CID2							

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UARTPCellID3, type RO, offset 0xFFC, reset 0x0000.00B1 (see page 746)															
								CID3							
Synchronous Serial Interface (SSI) SSI0 base: 0x4000.8000 SSI1 base: 0x4000.9000															
SSICR0, type R/W, offset 0x000, reset 0x0000.0000 (see page 762)															
SCR								SPH	SPO	FRF		DSS			
SSICR1, type R/W, offset 0x004, reset 0x0000.0000 (see page 764)															
											EOT	SOD	MS	SSE	LBM
SSIDR, type R/W, offset 0x008, reset 0x0000.0000 (see page 766)															
DATA															
SSISR, type RO, offset 0x00C, reset 0x0000.0003 (see page 767)															
											BSY	RFF	RNE	TNF	TFE
SSICPSR, type R/W, offset 0x010, reset 0x0000.0000 (see page 769)															
								CPSDVSR							
SSIIM, type R/W, offset 0x014, reset 0x0000.0000 (see page 770)															
												TXIM	RXIM	RTIM	RORIM
SSIRIS, type RO, offset 0x018, reset 0x0000.0008 (see page 771)															
												TXRIS	RXRIS	RTRIS	RORRIS
SSIMIS, type RO, offset 0x01C, reset 0x0000.0000 (see page 773)															
												TXMIS	RXMIS	RTMIS	RORMIS
SSIICR, type W1C, offset 0x020, reset 0x0000.0000 (see page 775)															
														RTIC	RORIC
SSIDMACTL, type R/W, offset 0x024, reset 0x0000.0000 (see page 776)															
														TXDMAE	RXDMAE
SSIPeriphID4, type RO, offset 0xFD0, reset 0x0000.0000 (see page 777)															
								PID4							
SSIPeriphID5, type RO, offset 0xFD4, reset 0x0000.0000 (see page 778)															
								PID5							
SSIPeriphID6, type RO, offset 0xFD8, reset 0x0000.0000 (see page 779)															
								PID6							
SSIPeriphID7, type RO, offset 0xFDC, reset 0x0000.0000 (see page 780)															
								PID7							
SSIPeriphID0, type RO, offset 0xFE0, reset 0x0000.0022 (see page 781)															
								PID0							

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSIPeriphID1, type RO, offset 0xFE4, reset 0x0000.0000 (see page 782)															
								PID1							
SSIPeriphID2, type RO, offset 0xFE8, reset 0x0000.0018 (see page 783)															
								PID2							
SSIPeriphID3, type RO, offset 0xFEC, reset 0x0000.0001 (see page 784)															
								PID3							
SSIPCellID0, type RO, offset 0xFF0, reset 0x0000.000D (see page 785)															
								CID0							
SSIPCellID1, type RO, offset 0xFF4, reset 0x0000.00F0 (see page 786)															
								CID1							
SSIPCellID2, type RO, offset 0xFF8, reset 0x0000.0005 (see page 787)															
								CID2							
SSIPCellID3, type RO, offset 0xFFC, reset 0x0000.00B1 (see page 788)															
								CID3							
Inter-Integrated Circuit (I²C) Interface **I²C Master** I2C 0 base: 0x4002.0000 I2C 1 base: 0x4002.1000															
I2CMSA, type R/W, offset 0x000, reset 0x0000.0000															
								SA							R/S
I2CMCS, type RO, offset 0x004, reset 0x0000.0020 (Read-Only Status Register)															
									BUSBSY	IDLE	ARBLST	DATACK	ADRACK	ERROR	BUSY
I2CMCS, type WO, offset 0x004, reset 0x0000.0020 (Write-Only Control Register)															
												ACK	STOP	START	RUN
I2CMDR, type R/W, offset 0x008, reset 0x0000.0000															
								DATA							
I2CMTPR, type R/W, offset 0x00C, reset 0x0000.0001															
									TPR						
I2CMIMR, type R/W, offset 0x010, reset 0x0000.0000															
															IM
I2CMRIS, type RO, offset 0x014, reset 0x0000.0000															
															RIS
I2CMMIS, type RO, offset 0x018, reset 0x0000.0000															
															MIS
I2CMICR, type WO, offset 0x01C, reset 0x0000.0000															
															IC

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I2CMCR, type R/W, offset 0x020, reset 0x0000.0000															
										SFE	MFE				LPBK
Inter-Integrated Circuit (I^2C) Interface **I^2C Slave** I2C 0 base: 0x4002.0000 I2C 1 base: 0x4002.1000															
I2CSOAR, type R/W, offset 0x800, reset 0x0000.0000															
									OAR						
I2CSCSR, type RO, offset 0x804, reset 0x0000.0000 (Read-Only Status Register)															
													FBR	TREQ	RREQ
I2CSCSR, type WO, offset 0x804, reset 0x0000.0000 (Write-Only Control Register)															
															DA
I2CSDR, type R/W, offset 0x808, reset 0x0000.0000															
								DATA							
I2CSIMR, type R/W, offset 0x80C, reset 0x0000.0000															
													STOPIM	STARTIM	DATAIM
I2CSRIS, type RO, offset 0x810, reset 0x0000.0000															
													STOPRIS	STARTRIS	DATARIS
I2CSMIS, type RO, offset 0x814, reset 0x0000.0000															
													STOPMIS	STARTMIS	DATAMIS
I2CSICR, type WO, offset 0x818, reset 0x0000.0000															
													STOPIC	STARTIC	DATAIC
Inter-Integrated Circuit Sound (I^2S) Interface Base 0x4005.4000															
I2STXFIFO, type WO, offset 0x000, reset 0x0000.0000 (see page 840)															
TXFIFO															
TXFIFO															
I2STXFIFOCFG, type R/W, offset 0x004, reset 0x0000.0000 (see page 841)															
														CSS	LRS
I2STXCFG, type R/W, offset 0x008, reset 0x1400.7DF0 (see page 842)															
		JST	DLY	SCP	LRP	WM		FMT	MSL						
SSZ				SDSZ											
I2STXLIMIT, type R/W, offset 0x00C, reset 0x0000.0000 (see page 844)															
											LIMIT				
I2STXISM, type R/W, offset 0x010, reset 0x0000.0000 (see page 845)															
															FFI
															FFM
I2STXLEV, type RO, offset 0x018, reset 0x0000.0000 (see page 846)															
											LEVEL				

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I2SRXFIFO, type RO, offset 0x800, reset 0x0000.0000 (see page 847)															
RXFIFO															
RXFIFO															
I2SRXFIFOCFG, type R/W, offset 0x804, reset 0x0000.0000 (see page 848)															
													FMM	CSS	LRS
I2SRXCFG, type R/W, offset 0x808, reset 0x1400.7DF0 (see page 849)															
		JST	DLY	SCP	LRP		RM		MSL						
SSZ						SDSZ									
I2SRXLIMIT, type R/W, offset 0x80C, reset 0x0000.7FFF (see page 852)															
											LIMIT				
I2SRXISM, type R/W, offset 0x810, reset 0x0000.0000 (see page 853)															
															FFI
															FFM
I2SRXLEV, type RO, offset 0x818, reset 0x0000.0000 (see page 854)															
											LEVEL				
I2SCFG, type R/W, offset 0xC00, reset 0x0000.0000 (see page 855)															
										RXSLV	TXSLV			RXEN	TXEN
I2SIM, type R/W, offset 0xC10, reset 0x0000.0000 (see page 857)															
										RXREIM	RXSRIM			TXWEIM	TXSRIM
I2SRIS, type RO, offset 0xC14, reset 0x0000.0000 (see page 859)															
										RXRERIS	RXSRRIS			TXWERIS	TXSRRIS
I2SMIS, type RO, offset 0xC18, reset 0x0000.0000 (see page 861)															
										RXREMIS	RXSRMIS			TXWEMIS	TXSRMIS
I2SIC, type WO, offset 0xC1C, reset 0x0000.0000 (see page 863)															
										RXREIC				TXWEIC	
Controller Area Network (CAN) Module CAN0 base: 0x4004.0000 CAN1 base: 0x4004.1000															
CANCTL, type R/W, offset 0x000, reset 0x0000.0001 (see page 886)															
								TEST	CCE	DAR		EIE	SIE	IE	INIT
CANSTS, type R/W, offset 0x004, reset 0x0000.0000 (see page 888)															
								BOFF	EWARN	EPASS	RXOK	TXOK	LEC		
CANERR, type RO, offset 0x008, reset 0x0000.0000 (see page 891)															
RP	REC							TEC							
CANBIT, type R/W, offset 0x00C, reset 0x0000.2301 (see page 892)															
	TSEG2			TSEG1				SJW		BRP					
CANINT, type RO, offset 0x010, reset 0x0000.0000 (see page 893)															
INTID															

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CANTST, type R/W, offset 0x014, reset 0x0000.0000 (see page 894)															
								RX	TX		LBACK	SILENT	BASIC		
CANBRPE, type R/W, offset 0x018, reset 0x0000.0000 (see page 896)															
												BRPE			
CANIF1CRQ, type R/W, offset 0x020, reset 0x0000.0001 (see page 897)															
BUSY										MNUM					
CANIF2CRQ, type R/W, offset 0x080, reset 0x0000.0001 (see page 897)															
BUSY										MNUM					
CANIF1CMSK, type R/W, offset 0x024, reset 0x0000.0000 (see page 898)															
								WRNRD	MASK	ARB	CONTROL	CLRINTPND	NEWDAT / TXRQST	DATAA	DATAB
CANIF2CMSK, type R/W, offset 0x084, reset 0x0000.0000 (see page 898)															
								WRNRD	MASK	ARB	CONTROL	CLRINTPND	NEWDAT / TXRQST	DATAA	DATAB
CANIF1MSK1, type R/W, offset 0x028, reset 0x0000.FFFF (see page 901)															
MSK															
CANIF2MSK1, type R/W, offset 0x088, reset 0x0000.FFFF (see page 901)															
MSK															
CANIF1MSK2, type R/W, offset 0x02C, reset 0x0000.FFFF (see page 902)															
MXTD	MDIR		MSK												
CANIF2MSK2, type R/W, offset 0x08C, reset 0x0000.FFFF (see page 902)															
MXTD	MDIR		MSK												
CANIF1ARB1, type R/W, offset 0x030, reset 0x0000.0000 (see page 904)															
ID															
CANIF2ARB1, type R/W, offset 0x090, reset 0x0000.0000 (see page 904)															
ID															
CANIF1ARB2, type R/W, offset 0x034, reset 0x0000.0000 (see page 905)															
MSGVAL	XTD	DIR	ID												
CANIF2ARB2, type R/W, offset 0x094, reset 0x0000.0000 (see page 905)															
MSGVAL	XTD	DIR	ID												
CANIF1MCTL, type R/W, offset 0x038, reset 0x0000.0000 (see page 907)															
NEWDAT	MSGLST	INTPND	UMASK	TXIE	RXIE	RMTEN	TXRQST	EOB				DLC			
CANIF2MCTL, type R/W, offset 0x098, reset 0x0000.0000 (see page 907)															
NEWDAT	MSGLST	INTPND	UMASK	TXIE	RXIE	RMTEN	TXRQST	EOB				DLC			
CANIF1DA1, type R/W, offset 0x03C, reset 0x0000.0000 (see page 910)															
DATA															

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CANIF1DA2, type R/W, offset 0x040, reset 0x0000.0000 (see page 910)															
DATA															
CANIF1DB1, type R/W, offset 0x044, reset 0x0000.0000 (see page 910)															
DATA															
CANIF1DB2, type R/W, offset 0x048, reset 0x0000.0000 (see page 910)															
DATA															
CANIF2DA1, type R/W, offset 0x09C, reset 0x0000.0000 (see page 910)															
DATA															
CANIF2DA2, type R/W, offset 0x0A0, reset 0x0000.0000 (see page 910)															
DATA															
CANIF2DB1, type R/W, offset 0x0A4, reset 0x0000.0000 (see page 910)															
DATA															
CANIF2DB2, type R/W, offset 0x0A8, reset 0x0000.0000 (see page 910)															
DATA															
CANTXRQ1, type RO, offset 0x100, reset 0x0000.0000 (see page 911)															
TXRQST															
CANTXRQ2, type RO, offset 0x104, reset 0x0000.0000 (see page 911)															
TXRQST															
CANNWDA1, type RO, offset 0x120, reset 0x0000.0000 (see page 912)															
NEWDAT															
CANNWDA2, type RO, offset 0x124, reset 0x0000.0000 (see page 912)															
NEWDAT															
CANMSG1INT, type RO, offset 0x140, reset 0x0000.0000 (see page 913)															
INTPND															
CANMSG2INT, type RO, offset 0x144, reset 0x0000.0000 (see page 913)															
INTPND															
CANMSG1VAL, type RO, offset 0x160, reset 0x0000.0000 (see page 914)															
MSGVAL															
CANMSG2VAL, type RO, offset 0x164, reset 0x0000.0000 (see page 914)															
MSGVAL															
Ethernet Controller **Ethernet MAC (Ethernet Offset)** Base 0x4004.8000															
MACRIS/MACIACK, type R/W1C, offset 0x000, reset 0x0000.0000															
									PHYINT	MDINT	RXER	FOV	TXEMP	TXER	RXINT

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MACIM, type R/W, offset 0x004, reset 0x0000.007F															
									PHYINTM	MDINTM	RXERM	FOVM	TXEMPM	TXERM	RXINTM
MACRCTL, type R/W, offset 0x008, reset 0x0000.0008															
											RSTFIFO	BADCRC	PRMS	AMUL	RXEN
MACTCTL, type R/W, offset 0x00C, reset 0x0000.0000															
											DUPLEX		CRC	PADEN	TXEN
MACDATA, type RO, offset 0x010, reset 0x0000.0000 (Reads)															
RXDATA															
RXDATA															
MACDATA, type WO, offset 0x010, reset 0x0000.0000 (Writes)															
TXDATA															
TXDATA															
MACIA0, type R/W, offset 0x014, reset 0x0000.0000															
MACOCT4								MACOCT3							
MACOCT2								MACOCT1							
MACIA1, type R/W, offset 0x018, reset 0x0000.0000															
MACOCT6								MACOCT5							
MACTHR, type R/W, offset 0x01C, reset 0x0000.003F															
										THRESH					
MACMCTL, type R/W, offset 0x020, reset 0x0000.0000															
								REGADR						WRITE	START
MACMDV, type R/W, offset 0x024, reset 0x0000.0080															
								DIV							
MACMTXD, type R/W, offset 0x02C, reset 0x0000.0000															
MDTX															
MACMRXD, type R/W, offset 0x030, reset 0x0000.0000															
MDRX															
MACNP, type RO, offset 0x034, reset 0x0000.0000															
										NPR					
MACTR, type R/W, offset 0x038, reset 0x0000.0000															
															NEWTX
MACTS, type R/W, offset 0x03C, reset 0x0000.0000															
															TSEN
MACLED, type R/W, offset 0x040, reset 0x0000.0100															
				LED1								LED0			
MDIX, type R/W, offset 0x044, reset 0x0000.0000															
															EN

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Ethernet Controller **MII Management (Accessed through the MACMCTL register)**															
MR0, type R/W, address 0x00, reset 0x1000															
RESET	LOOPBK	SPEEDSL	ANEGEN	PWRDN	ISO	RANEG	DUPLEX	COLT							
MR1, type RO, address 0x01, reset 0x7809															
	100X_F	100X_H	10T_F	10T_H						ANEGC	RFAULT	ANEGA	LINK	JAB	EXTD
MR2, type RO, address 0x02, reset 0x0161															
OUI[21:6]															
MR3, type RO, address 0x03, reset 0xB410															
OUI[5:0]						MN						RN			
MR4, type R/W, address 0x04, reset 0x01E1															
NP		RF					A3	A2	A1	A0	S				
MR5, type RO, address 0x05, reset 0x0001															
NP	ACK	RF	A								S				
MR6, type RO, address 0x06, reset 0x0000															
											PDF	LPNPA		PRX	LPANEGA
MR16, type RO, address 0x10, reset 0x0040															
						SR									
MR17, type R/W, address 0x11, reset 0x0002															
	FASTRIP	EDPD		LSQE			FASTEST						FGLS	ENON	
MR27, type RO, address 0x1B, reset -															
											XPOL				
MR29, type RO, address 0x1D, reset 0x0000															
								EONIS	ANCOMPIS	RFLTIS	LDIS	LPACKIS	PDFIS	PRXIS	
MR30, type R/W, address 0x1E, reset 0x0000															
								EONIM	ANCOMPIM	RFLTIM	LDIM	LPACKIM	PDFIM	PRXIM	
MR31, type R/W, address 0x1F, reset 0x0040															
			AUTODONE								SPEED				SCRDIS
Universal Serial Bus (USB) Controller Base 0x4005.0000															
USBFADDR, type R/W, offset 0x000, reset 0x00 (see page 1004)															
									FUNCADDR						
USBPOWER, type R/W, offset 0x001, reset 0x20 (OTG A / Host Mode) (see page 1005)															
												RESET	RESUME	SUSPEND	PWRDNPHY
USBPOWER, type R/W, offset 0x001, reset 0x20 (OTG B / Device Mode) (see page 1005)															
								ISOUP	SOFTCONN			RESET	RESUME	SUSPEND	PWRDNPHY
USBTXIS, type RO, offset 0x002, reset 0x0000 (see page 1008)															
EP15	EP14	EP13	EP12	EP11	EP10	EP9	EP8	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0
USBRXIS, type RO, offset 0x004, reset 0x0000 (see page 1010)															
EP15	EP14	EP13	EP12	EP11	EP10	EP9	EP8	EP7	EP6	EP5	EP4	EP3	EP2	EP1	
USBTXIE, type R/W, offset 0x006, reset 0xFFFF (see page 1012)															
EP15	EP14	EP13	EP12	EP11	EP10	EP9	EP8	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0
USBRXIE, type R/W, offset 0x008, reset 0xFFFE (see page 1014)															
EP15	EP14	EP13	EP12	EP11	EP10	EP9	EP8	EP7	EP6	EP5	EP4	EP3	EP2	EP1	
USBIS, type RO, offset 0x00A, reset 0x00 (OTG A / Host Mode) (see page 1016)															
								VBUSERR	SESREQ	DISCON	CONN	SOF	BABBLE	RESUME	
USBIS, type RO, offset 0x00A, reset 0x00 (OTG B / Device Mode) (see page 1016)															
										DISCON		SOF	RESET	RESUME	SUSPEND
USBIE, type R/W, offset 0x00B, reset 0x06 (OTG A / Host Mode) (see page 1019)															
								VBUSERR	SESREQ	DISCON	CONN	SOF	BABBLE	RESUME	

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USBIE, type R/W, offset 0x00B, reset 0x06 (OTG B / Device Mode) (see page 1019)															
										DISCON		SOF	RESET	RESUME	SUSPEND
USBFRAME, type RO, offset 0x00C, reset 0x0000 (see page 1022)															
					FRAME										
USBEPIDX, type R/W, offset 0x00E, reset 0x00 (see page 1023)															
												EPIDX			
USBTEST, type R/W, offset 0x00F, reset 0x00 (OTG A / Host Mode) (see page 1024)															
								FORCEH	FIFOACC	FORCEFS					
USBTEST, type R/W, offset 0x00F, reset 0x00 (OTG B / Device Mode) (see page 1024)															
									FIFOACC	FORCEFS					
USBFIFO0, type R/W, offset 0x020, reset 0x0000.0000 (see page 1026)															
								EPDATA							
								EPDATA							
USBFIFO1, type R/W, offset 0x024, reset 0x0000.0000 (see page 1026)															
								EPDATA							
								EPDATA							
USBFIFO2, type R/W, offset 0x028, reset 0x0000.0000 (see page 1026)															
								EPDATA							
								EPDATA							
USBFIFO3, type R/W, offset 0x02C, reset 0x0000.0000 (see page 1026)															
								EPDATA							
								EPDATA							
USBFIFO4, type R/W, offset 0x030, reset 0x0000.0000 (see page 1026)															
								EPDATA							
								EPDATA							
USBFIFO5, type R/W, offset 0x034, reset 0x0000.0000 (see page 1026)															
								EPDATA							
								EPDATA							
USBFIFO6, type R/W, offset 0x038, reset 0x0000.0000 (see page 1026)															
								EPDATA							
								EPDATA							
USBFIFO7, type R/W, offset 0x03C, reset 0x0000.0000 (see page 1026)															
								EPDATA							
								EPDATA							
USBFIFO8, type R/W, offset 0x040, reset 0x0000.0000 (see page 1026)															
								EPDATA							
								EPDATA							
USBFIFO9, type R/W, offset 0x044, reset 0x0000.0000 (see page 1026)															
								EPDATA							
								EPDATA							
USBFIFO10, type R/W, offset 0x048, reset 0x0000.0000 (see page 1026)															
								EPDATA							
								EPDATA							
USBFIFO11, type R/W, offset 0x04C, reset 0x0000.0000 (see page 1026)															
								EPDATA							
								EPDATA							
USBFIFO12, type R/W, offset 0x050, reset 0x0000.0000 (see page 1026)															
								EPDATA							
								EPDATA							
USBFIFO13, type R/W, offset 0x054, reset 0x0000.0000 (see page 1026)															
								EPDATA							
								EPDATA							

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USBFIFO14, type R/W, offset 0x058, reset 0x0000.0000 (see page 1026)															
EPDATA															
EPDATA															
USBFIFO15, type R/W, offset 0x05C, reset 0x0000.0000 (see page 1026)															
EPDATA															
EPDATA															
USBDEVCTL, type R/W, offset 0x060, reset 0x80 (see page 1028)															
								DEV	FSDEV	LSDEV	VBUS		HOST	HOSTREQ	SESSION
USBTXFIFOSZ, type R/W, offset 0x062, reset 0x00 (see page 1030)															
											DPB	SIZE			
USBRXFIFOSZ, type R/W, offset 0x063, reset 0x00 (see page 1030)															
											DPB	SIZE			
USBTXFIFOADD, type R/W, offset 0x064, reset 0x0000 (see page 1031)															
							ADDR								
USBRXFIFOADD, type R/W, offset 0x066, reset 0x0000 (see page 1031)															
							ADDR								
USBCONTIM, type R/W, offset 0x07A, reset 0x5C (see page 1032)															
								WTCON				WTID			
USBVPLEN, type R/W, offset 0x07B, reset 0x3C (see page 1033)															
								VPLEN							
USBFSEOF, type R/W, offset 0x07D, reset 0x77 (see page 1034)															
								FSEOFG							
USBLSEOF, type R/W, offset 0x07E, reset 0x72 (see page 1035)															
								LSEOFG							
USBTXFUNCADDR0, type R/W, offset 0x080, reset 0x00 (see page 1036)															
									ADDR						
USBTXFUNCADDR1, type R/W, offset 0x088, reset 0x00 (see page 1036)															
									ADDR						
USBTXFUNCADDR2, type R/W, offset 0x090, reset 0x00 (see page 1036)															
									ADDR						
USBTXFUNCADDR3, type R/W, offset 0x098, reset 0x00 (see page 1036)															
									ADDR						
USBTXFUNCADDR4, type R/W, offset 0x0A0, reset 0x00 (see page 1036)															
									ADDR						
USBTXFUNCADDR5, type R/W, offset 0x0A8, reset 0x00 (see page 1036)															
									ADDR						
USBTXFUNCADDR6, type R/W, offset 0x0B0, reset 0x00 (see page 1036)															
									ADDR						
USBTXFUNCADDR7, type R/W, offset 0x0B8, reset 0x00 (see page 1036)															
									ADDR						
USBTXFUNCADDR8, type R/W, offset 0x0C0, reset 0x00 (see page 1036)															
									ADDR						
USBTXFUNCADDR9, type R/W, offset 0x0C8, reset 0x00 (see page 1036)															
									ADDR						
USBTXFUNCADDR10, type R/W, offset 0x0D0, reset 0x00 (see page 1036)															
									ADDR						
USBTXFUNCADDR11, type R/W, offset 0x0D8, reset 0x00 (see page 1036)															
									ADDR						
USBTXFUNCADDR12, type R/W, offset 0x0E0, reset 0x00 (see page 1036)															
									ADDR						
USBTXFUNCADDR13, type R/W, offset 0x0E8, reset 0x00 (see page 1036)															
									ADDR						

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USBTXFUNCADDR14, type R/W, offset 0x0F0, reset 0x00 (see page 1036)															
									ADDR						
USBTXFUNCADDR15, type R/W, offset 0x0F8, reset 0x00 (see page 1036)															
									ADDR						
USBTXHUBADDR0, type R/W, offset 0x082, reset 0x00 (see page 1038)															
									ADDR						
USBTXHUBADDR1, type R/W, offset 0x08A, reset 0x00 (see page 1038)															
									ADDR						
USBTXHUBADDR2, type R/W, offset 0x092, reset 0x00 (see page 1038)															
									ADDR						
USBTXHUBADDR3, type R/W, offset 0x09A, reset 0x00 (see page 1038)															
									ADDR						
USBTXHUBADDR4, type R/W, offset 0x0A2, reset 0x00 (see page 1038)															
									ADDR						
USBTXHUBADDR5, type R/W, offset 0x0AA, reset 0x00 (see page 1038)															
									ADDR						
USBTXHUBADDR6, type R/W, offset 0x0B2, reset 0x00 (see page 1038)															
									ADDR						
USBTXHUBADDR7, type R/W, offset 0x0BA, reset 0x00 (see page 1038)															
									ADDR						
USBTXHUBADDR8, type R/W, offset 0x0C2, reset 0x00 (see page 1038)															
									ADDR						
USBTXHUBADDR9, type R/W, offset 0x0CA, reset 0x00 (see page 1038)															
									ADDR						
USBTXHUBADDR10, type R/W, offset 0x0D2, reset 0x00 (see page 1038)															
									ADDR						
USBTXHUBADDR11, type R/W, offset 0x0DA, reset 0x00 (see page 1038)															
									ADDR						
USBTXHUBADDR12, type R/W, offset 0x0E2, reset 0x00 (see page 1038)															
									ADDR						
USBTXHUBADDR13, type R/W, offset 0x0EA, reset 0x00 (see page 1038)															
									ADDR						
USBTXHUBADDR14, type R/W, offset 0x0F2, reset 0x00 (see page 1038)															
									ADDR						
USBTXHUBADDR15, type R/W, offset 0x0FA, reset 0x00 (see page 1038)															
									ADDR						
USBTXHUBPORT0, type R/W, offset 0x083, reset 0x00 (see page 1040)															
									PORT						
USBTXHUBPORT1, type R/W, offset 0x08B, reset 0x00 (see page 1040)															
									PORT						
USBTXHUBPORT2, type R/W, offset 0x093, reset 0x00 (see page 1040)															
									PORT						
USBTXHUBPORT3, type R/W, offset 0x09B, reset 0x00 (see page 1040)															
									PORT						
USBTXHUBPORT4, type R/W, offset 0x0A3, reset 0x00 (see page 1040)															
									PORT						
USBTXHUBPORT5, type R/W, offset 0x0AB, reset 0x00 (see page 1040)															
									PORT						
USBTXHUBPORT6, type R/W, offset 0x0B3, reset 0x00 (see page 1040)															
									PORT						
USBTXHUBPORT7, type R/W, offset 0x0BB, reset 0x00 (see page 1040)															
									PORT						

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USBTXHUBPORT8, type R/W, offset 0x0C3, reset 0x00 (see page 1040)															
									PORT						
USBTXHUBPORT9, type R/W, offset 0x0CB, reset 0x00 (see page 1040)															
									PORT						
USBTXHUBPORT10, type R/W, offset 0x0D3, reset 0x00 (see page 1040)															
									PORT						
USBTXHUBPORT11, type R/W, offset 0x0DB, reset 0x00 (see page 1040)															
									PORT						
USBTXHUBPORT12, type R/W, offset 0x0E3, reset 0x00 (see page 1040)															
									PORT						
USBTXHUBPORT13, type R/W, offset 0x0EB, reset 0x00 (see page 1040)															
									PORT						
USBTXHUBPORT14, type R/W, offset 0x0F3, reset 0x00 (see page 1040)															
									PORT						
USBTXHUBPORT15, type R/W, offset 0x0FB, reset 0x00 (see page 1040)															
									PORT						
USBRXFUNCADDR1, type R/W, offset 0x08C, reset 0x00 (see page 1042)															
									ADDR						
USBRXFUNCADDR2, type R/W, offset 0x094, reset 0x00 (see page 1042)															
									ADDR						
USBRXFUNCADDR3, type R/W, offset 0x09C, reset 0x00 (see page 1042)															
									ADDR						
USBRXFUNCADDR4, type R/W, offset 0x0A4, reset 0x00 (see page 1042)															
									ADDR						
USBRXFUNCADDR5, type R/W, offset 0x0AC, reset 0x00 (see page 1042)															
									ADDR						
USBRXFUNCADDR6, type R/W, offset 0x0B4, reset 0x00 (see page 1042)															
									ADDR						
USBRXFUNCADDR7, type R/W, offset 0x0BC, reset 0x00 (see page 1042)															
									ADDR						
USBRXFUNCADDR8, type R/W, offset 0x0C4, reset 0x00 (see page 1042)															
									ADDR						
USBRXFUNCADDR9, type R/W, offset 0x0CC, reset 0x00 (see page 1042)															
									ADDR						
USBRXFUNCADDR10, type R/W, offset 0x0D4, reset 0x00 (see page 1042)															
									ADDR						
USBRXFUNCADDR11, type R/W, offset 0x0DC, reset 0x00 (see page 1042)															
									ADDR						
USBRXFUNCADDR12, type R/W, offset 0x0E4, reset 0x00 (see page 1042)															
									ADDR						
USBRXFUNCADDR13, type R/W, offset 0x0EC, reset 0x00 (see page 1042)															
									ADDR						
USBRXFUNCADDR14, type R/W, offset 0x0F4, reset 0x00 (see page 1042)															
									ADDR						
USBRXFUNCADDR15, type R/W, offset 0x0FC, reset 0x00 (see page 1042)															
									ADDR						
USBRXHUBADDR1, type R/W, offset 0x08E, reset 0x00 (see page 1044)															
									ADDR						
USBRXHUBADDR2, type R/W, offset 0x096, reset 0x00 (see page 1044)															
									ADDR						
USBRXHUBADDR3, type R/W, offset 0x09E, reset 0x00 (see page 1044)															
									ADDR						

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USBRXHUBADDR4, type R/W, offset 0x0A6, reset 0x00 (see page 1044)															
									ADDR						
USBRXHUBADDR5, type R/W, offset 0x0AE, reset 0x00 (see page 1044)															
									ADDR						
USBRXHUBADDR6, type R/W, offset 0x0B6, reset 0x00 (see page 1044)															
									ADDR						
USBRXHUBADDR7, type R/W, offset 0x0BE, reset 0x00 (see page 1044)															
									ADDR						
USBRXHUBADDR8, type R/W, offset 0x0C6, reset 0x00 (see page 1044)															
									ADDR						
USBRXHUBADDR9, type R/W, offset 0x0CE, reset 0x00 (see page 1044)															
									ADDR						
USBRXHUBADDR10, type R/W, offset 0x0D6, reset 0x00 (see page 1044)															
									ADDR						
USBRXHUBADDR11, type R/W, offset 0x0DE, reset 0x00 (see page 1044)															
									ADDR						
USBRXHUBADDR12, type R/W, offset 0x0E6, reset 0x00 (see page 1044)															
									ADDR						
USBRXHUBADDR13, type R/W, offset 0x0EE, reset 0x00 (see page 1044)															
									ADDR						
USBRXHUBADDR14, type R/W, offset 0x0F6, reset 0x00 (see page 1044)															
									ADDR						
USBRXHUBADDR15, type R/W, offset 0x0FE, reset 0x00 (see page 1044)															
									ADDR						
USBRXHUBPORT1, type R/W, offset 0x08F, reset 0x00 (see page 1046)															
									PORT						
USBRXHUBPORT2, type R/W, offset 0x097, reset 0x00 (see page 1046)															
									PORT						
USBRXHUBPORT3, type R/W, offset 0x09F, reset 0x00 (see page 1046)															
									PORT						
USBRXHUBPORT4, type R/W, offset 0x0A7, reset 0x00 (see page 1046)															
									PORT						
USBRXHUBPORT5, type R/W, offset 0x0AF, reset 0x00 (see page 1046)															
									PORT						
USBRXHUBPORT6, type R/W, offset 0x0B7, reset 0x00 (see page 1046)															
									PORT						
USBRXHUBPORT7, type R/W, offset 0x0BF, reset 0x00 (see page 1046)															
									PORT						
USBRXHUBPORT8, type R/W, offset 0x0C7, reset 0x00 (see page 1046)															
									PORT						
USBRXHUBPORT9, type R/W, offset 0x0CF, reset 0x00 (see page 1046)															
									PORT						
USBRXHUBPORT10, type R/W, offset 0x0D7, reset 0x00 (see page 1046)															
									PORT						
USBRXHUBPORT11, type R/W, offset 0x0DF, reset 0x00 (see page 1046)															
									PORT						
USBRXHUBPORT12, type R/W, offset 0x0E7, reset 0x00 (see page 1046)															
									PORT						
USBRXHUBPORT13, type R/W, offset 0x0EF, reset 0x00 (see page 1046)															
									PORT						
USBRXHUBPORT14, type R/W, offset 0x0F7, reset 0x00 (see page 1046)															
									PORT						

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USBRXHUBPORT15, type R/W, offset 0x0FF, reset 0x00 (see page 1046)															
									PORT						
USBTXMAXP1, type R/W, offset 0x110, reset 0x0000 (see page 1048)															
					MAXLOAD										
USBTXMAXP2, type R/W, offset 0x120, reset 0x0000 (see page 1048)															
					MAXLOAD										
USBTXMAXP3, type R/W, offset 0x130, reset 0x0000 (see page 1048)															
					MAXLOAD										
USBTXMAXP4, type R/W, offset 0x140, reset 0x0000 (see page 1048)															
					MAXLOAD										
USBTXMAXP5, type R/W, offset 0x150, reset 0x0000 (see page 1048)															
					MAXLOAD										
USBTXMAXP6, type R/W, offset 0x160, reset 0x0000 (see page 1048)															
					MAXLOAD										
USBTXMAXP7, type R/W, offset 0x170, reset 0x0000 (see page 1048)															
					MAXLOAD										
USBTXMAXP8, type R/W, offset 0x180, reset 0x0000 (see page 1048)															
					MAXLOAD										
USBTXMAXP9, type R/W, offset 0x190, reset 0x0000 (see page 1048)															
					MAXLOAD										
USBTXMAXP10, type R/W, offset 0x1A0, reset 0x0000 (see page 1048)															
					MAXLOAD										
USBTXMAXP11, type R/W, offset 0x1B0, reset 0x0000 (see page 1048)															
					MAXLOAD										
USBTXMAXP12, type R/W, offset 0x1C0, reset 0x0000 (see page 1048)															
					MAXLOAD										
USBTXMAXP13, type R/W, offset 0x1D0, reset 0x0000 (see page 1048)															
					MAXLOAD										
USBTXMAXP14, type R/W, offset 0x1E0, reset 0x0000 (see page 1048)															
					MAXLOAD										
USBTXMAXP15, type R/W, offset 0x1F0, reset 0x0000 (see page 1048)															
					MAXLOAD										
USBCSRL0, type W1C, offset 0x102, reset 0x00 (OTG A / Host Mode) (see page 1050)															
								NAKTO	STATUS	REQPKT	ERROR	SETUP	STALLED	TXRDY	RXRDY
USBCSRL0, type W1C, offset 0x102, reset 0x00 (OTG B / Device Mode) (see page 1050)															
								SETENDC	RXRDYC	STALL	SETEND	DATAEND	STALLED	TXRDY	RXRDY
USBCSRH0, type W1C, offset 0x103, reset 0x00 (OTG A / Host Mode) (see page 1054)															
													DTWE	DT	FLUSH
USBCSRH0, type W1C, offset 0x103, reset 0x00 (OTG B / Device Mode) (see page 1054)															
															FLUSH
USBCOUNT0, type RO, offset 0x108, reset 0x00 (see page 1056)															
									COUNT						
USBTYPE0, type R/W, offset 0x10A, reset 0x00 (see page 1057)															
								SPEED							
USBNAKLMT, type R/W, offset 0x10B, reset 0x00 (see page 1058)															
											NAKLMT				
USBTXCSRL1, type R/W, offset 0x112, reset 0x00 (OTG A / Host Mode) (see page 1059)															
								NAKTO	CLRDT	STALLED	SETUP	FLUSH	ERROR	FIFONE	TXRDY
USBTXCSRL2, type R/W, offset 0x122, reset 0x00 (OTG A / Host Mode) (see page 1059)															
								NAKTO	CLRDT	STALLED	SETUP	FLUSH	ERROR	FIFONE	TXRDY
USBTXCSRL3, type R/W, offset 0x132, reset 0x00 (OTG A / Host Mode) (see page 1059)															
								NAKTO	CLRDT	STALLED	SETUP	FLUSH	ERROR	FIFONE	TXRDY

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USBTXCSRL4, type R/W, offset 0x142, reset 0x00 (OTG A / Host Mode) (see page 1059)															
								NAKTO	CLRDT	STALLED	SETUP	FLUSH	ERROR	FIFONE	TXRDY
USBTXCSRL5, type R/W, offset 0x152, reset 0x00 (OTG A / Host Mode) (see page 1059)															
								NAKTO	CLRDT	STALLED	SETUP	FLUSH	ERROR	FIFONE	TXRDY
USBTXCSRL6, type R/W, offset 0x162, reset 0x00 (OTG A / Host Mode) (see page 1059)															
								NAKTO	CLRDT	STALLED	SETUP	FLUSH	ERROR	FIFONE	TXRDY
USBTXCSRL7, type R/W, offset 0x172, reset 0x00 (OTG A / Host Mode) (see page 1059)															
								NAKTO	CLRDT	STALLED	SETUP	FLUSH	ERROR	FIFONE	TXRDY
USBTXCSRL8, type R/W, offset 0x182, reset 0x00 (OTG A / Host Mode) (see page 1059)															
								NAKTO	CLRDT	STALLED	SETUP	FLUSH	ERROR	FIFONE	TXRDY
USBTXCSRL9, type R/W, offset 0x192, reset 0x00 (OTG A / Host Mode) (see page 1059)															
								NAKTO	CLRDT	STALLED	SETUP	FLUSH	ERROR	FIFONE	TXRDY
USBTXCSRL10, type R/W, offset 0x1A2, reset 0x00 (OTG A / Host Mode) (see page 1059)															
								NAKTO	CLRDT	STALLED	SETUP	FLUSH	ERROR	FIFONE	TXRDY
USBTXCSRL11, type R/W, offset 0x1B2, reset 0x00 (OTG A / Host Mode) (see page 1059)															
								NAKTO	CLRDT	STALLED	SETUP	FLUSH	ERROR	FIFONE	TXRDY
USBTXCSRL12, type R/W, offset 0x1C2, reset 0x00 (OTG A / Host Mode) (see page 1059)															
								NAKTO	CLRDT	STALLED	SETUP	FLUSH	ERROR	FIFONE	TXRDY
USBTXCSRL13, type R/W, offset 0x1D2, reset 0x00 (OTG A / Host Mode) (see page 1059)															
								NAKTO	CLRDT	STALLED	SETUP	FLUSH	ERROR	FIFONE	TXRDY
USBTXCSRL14, type R/W, offset 0x1E2, reset 0x00 (OTG A / Host Mode) (see page 1059)															
								NAKTO	CLRDT	STALLED	SETUP	FLUSH	ERROR	FIFONE	TXRDY
USBTXCSRL15, type R/W, offset 0x1F2, reset 0x00 (OTG A / Host Mode) (see page 1059)															
								NAKTO	CLRDT	STALLED	SETUP	FLUSH	ERROR	FIFONE	TXRDY
USBTXCSRL1, type R/W, offset 0x112, reset 0x00 (OTG B / Device Mode) (see page 1059)															
									CLRDT	STALLED	STALL	FLUSH	UNDRN	FIFONE	TXRDY
USBTXCSRL2, type R/W, offset 0x122, reset 0x00 (OTG B / Device Mode) (see page 1059)															
									CLRDT	STALLED	STALL	FLUSH	UNDRN	FIFONE	TXRDY
USBTXCSRL3, type R/W, offset 0x132, reset 0x00 (OTG B / Device Mode) (see page 1059)															
									CLRDT	STALLED	STALL	FLUSH	UNDRN	FIFONE	TXRDY
USBTXCSRL4, type R/W, offset 0x142, reset 0x00 (OTG B / Device Mode) (see page 1059)															
									CLRDT	STALLED	STALL	FLUSH	UNDRN	FIFONE	TXRDY
USBTXCSRL5, type R/W, offset 0x152, reset 0x00 (OTG B / Device Mode) (see page 1059)															
									CLRDT	STALLED	STALL	FLUSH	UNDRN	FIFONE	TXRDY
USBTXCSRL6, type R/W, offset 0x162, reset 0x00 (OTG B / Device Mode) (see page 1059)															
									CLRDT	STALLED	STALL	FLUSH	UNDRN	FIFONE	TXRDY
USBTXCSRL7, type R/W, offset 0x172, reset 0x00 (OTG B / Device Mode) (see page 1059)															
									CLRDT	STALLED	STALL	FLUSH	UNDRN	FIFONE	TXRDY
USBTXCSRL8, type R/W, offset 0x182, reset 0x00 (OTG B / Device Mode) (see page 1059)															
									CLRDT	STALLED	STALL	FLUSH	UNDRN	FIFONE	TXRDY
USBTXCSRL9, type R/W, offset 0x192, reset 0x00 (OTG B / Device Mode) (see page 1059)															
									CLRDT	STALLED	STALL	FLUSH	UNDRN	FIFONE	TXRDY
USBTXCSRL10, type R/W, offset 0x1A2, reset 0x00 (OTG B / Device Mode) (see page 1059)															
									CLRDT	STALLED	STALL	FLUSH	UNDRN	FIFONE	TXRDY
USBTXCSRL11, type R/W, offset 0x1B2, reset 0x00 (OTG B / Device Mode) (see page 1059)															
									CLRDT	STALLED	STALL	FLUSH	UNDRN	FIFONE	TXRDY
USBTXCSRL12, type R/W, offset 0x1C2, reset 0x00 (OTG B / Device Mode) (see page 1059)															
									CLRDT	STALLED	STALL	FLUSH	UNDRN	FIFONE	TXRDY
USBTXCSRL13, type R/W, offset 0x1D2, reset 0x00 (OTG B / Device Mode) (see page 1059)															
									CLRDT	STALLED	STALL	FLUSH	UNDRN	FIFONE	TXRDY
USBTXCSRL14, type R/W, offset 0x1E2, reset 0x00 (OTG B / Device Mode) (see page 1059)															
									CLRDT	STALLED	STALL	FLUSH	UNDRN	FIFONE	TXRDY

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USBTXCSRL15, type R/W, offset 0x1F2, reset 0x00 (OTG B / Device Mode) (see page 1059)															
									CLRDT	STALLED	STALL	FLUSH	UNDRN	FIFONE	TXRDY
USBTXCSRH1, type R/W, offset 0x113, reset 0x00 (OTG A / Host Mode) (see page 1064)															
								AUTOSET		MODE	DMAEN	FDT	DMAMOD	DTWE	DT
USBTXCSRH2, type R/W, offset 0x123, reset 0x00 (OTG A / Host Mode) (see page 1064)															
								AUTOSET		MODE	DMAEN	FDT	DMAMOD	DTWE	DT
USBTXCSRH3, type R/W, offset 0x133, reset 0x00 (OTG A / Host Mode) (see page 1064)															
								AUTOSET		MODE	DMAEN	FDT	DMAMOD	DTWE	DT
USBTXCSRH4, type R/W, offset 0x143, reset 0x00 (OTG A / Host Mode) (see page 1064)															
								AUTOSET		MODE	DMAEN	FDT	DMAMOD	DTWE	DT
USBTXCSRH5, type R/W, offset 0x153, reset 0x00 (OTG A / Host Mode) (see page 1064)															
								AUTOSET		MODE	DMAEN	FDT	DMAMOD	DTWE	DT
USBTXCSRH6, type R/W, offset 0x163, reset 0x00 (OTG A / Host Mode) (see page 1064)															
								AUTOSET		MODE	DMAEN	FDT	DMAMOD	DTWE	DT
USBTXCSRH7, type R/W, offset 0x173, reset 0x00 (OTG A / Host Mode) (see page 1064)															
								AUTOSET		MODE	DMAEN	FDT	DMAMOD	DTWE	DT
USBTXCSRH8, type R/W, offset 0x183, reset 0x00 (OTG A / Host Mode) (see page 1064)															
								AUTOSET		MODE	DMAEN	FDT	DMAMOD	DTWE	DT
USBTXCSRH9, type R/W, offset 0x193, reset 0x00 (OTG A / Host Mode) (see page 1064)															
								AUTOSET		MODE	DMAEN	FDT	DMAMOD	DTWE	DT
USBTXCSRH10, type R/W, offset 0x1A3, reset 0x00 (OTG A / Host Mode) (see page 1064)															
								AUTOSET		MODE	DMAEN	FDT	DMAMOD	DTWE	DT
USBTXCSRH11, type R/W, offset 0x1B3, reset 0x00 (OTG A / Host Mode) (see page 1064)															
								AUTOSET		MODE	DMAEN	FDT	DMAMOD	DTWE	DT
USBTXCSRH12, type R/W, offset 0x1C3, reset 0x00 (OTG A / Host Mode) (see page 1064)															
								AUTOSET		MODE	DMAEN	FDT	DMAMOD	DTWE	DT
USBTXCSRH13, type R/W, offset 0x1D3, reset 0x00 (OTG A / Host Mode) (see page 1064)															
								AUTOSET		MODE	DMAEN	FDT	DMAMOD	DTWE	DT
USBTXCSRH14, type R/W, offset 0x1E3, reset 0x00 (OTG A / Host Mode) (see page 1064)															
								AUTOSET		MODE	DMAEN	FDT	DMAMOD	DTWE	DT
USBTXCSRH15, type R/W, offset 0x1F3, reset 0x00 (OTG A / Host Mode) (see page 1064)															
								AUTOSET		MODE	DMAEN	FDT	DMAMOD	DTWE	DT
USBTXCSRH1, type R/W, offset 0x113, reset 0x00 (OTG B / Device Mode) (see page 1064)															
								AUTOSET	ISO	MODE	DMAEN	FDT	DMAMOD		
USBTXCSRH2, type R/W, offset 0x123, reset 0x00 (OTG B / Device Mode) (see page 1064)															
								AUTOSET	ISO	MODE	DMAEN	FDT	DMAMOD		
USBTXCSRH3, type R/W, offset 0x133, reset 0x00 (OTG B / Device Mode) (see page 1064)															
								AUTOSET	ISO	MODE	DMAEN	FDT	DMAMOD		
USBTXCSRH4, type R/W, offset 0x143, reset 0x00 (OTG B / Device Mode) (see page 1064)															
								AUTOSET	ISO	MODE	DMAEN	FDT	DMAMOD		
USBTXCSRH5, type R/W, offset 0x153, reset 0x00 (OTG B / Device Mode) (see page 1064)															
								AUTOSET	ISO	MODE	DMAEN	FDT	DMAMOD		
USBTXCSRH6, type R/W, offset 0x163, reset 0x00 (OTG B / Device Mode) (see page 1064)															
								AUTOSET	ISO	MODE	DMAEN	FDT	DMAMOD		
USBTXCSRH7, type R/W, offset 0x173, reset 0x00 (OTG B / Device Mode) (see page 1064)															
								AUTOSET	ISO	MODE	DMAEN	FDT	DMAMOD		
USBTXCSRH8, type R/W, offset 0x183, reset 0x00 (OTG B / Device Mode) (see page 1064)															
								AUTOSET	ISO	MODE	DMAEN	FDT	DMAMOD		
USBTXCSRH9, type R/W, offset 0x193, reset 0x00 (OTG B / Device Mode) (see page 1064)															
								AUTOSET	ISO	MODE	DMAEN	FDT	DMAMOD		
USBTXCSRH10, type R/W, offset 0x1A3, reset 0x00 (OTG B / Device Mode) (see page 1064)															
								AUTOSET	ISO	MODE	DMAEN	FDT	DMAMOD		

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USBTXCSRH11, type R/W, offset 0x1B3, reset 0x00 (OTG B / Device Mode) (see page 1064)															
								AUTOSET	ISO	MODE	DMAEN	FDT	DMAMOD		
USBTXCSRH12, type R/W, offset 0x1C3, reset 0x00 (OTG B / Device Mode) (see page 1064)															
								AUTOSET	ISO	MODE	DMAEN	FDT	DMAMOD		
USBTXCSRH13, type R/W, offset 0x1D3, reset 0x00 (OTG B / Device Mode) (see page 1064)															
								AUTOSET	ISO	MODE	DMAEN	FDT	DMAMOD		
USBTXCSRH14, type R/W, offset 0x1E3, reset 0x00 (OTG B / Device Mode) (see page 1064)															
								AUTOSET	ISO	MODE	DMAEN	FDT	DMAMOD		
USBTXCSRH15, type R/W, offset 0x1F3, reset 0x00 (OTG B / Device Mode) (see page 1064)															
								AUTOSET	ISO	MODE	DMAEN	FDT	DMAMOD		
USBRXMAXP1, type R/W, offset 0x114, reset 0x0000 (see page 1068)															
					MAXLOAD										
USBRXMAXP2, type R/W, offset 0x124, reset 0x0000 (see page 1068)															
					MAXLOAD										
USBRXMAXP3, type R/W, offset 0x134, reset 0x0000 (see page 1068)															
					MAXLOAD										
USBRXMAXP4, type R/W, offset 0x144, reset 0x0000 (see page 1068)															
					MAXLOAD										
USBRXMAXP5, type R/W, offset 0x154, reset 0x0000 (see page 1068)															
					MAXLOAD										
USBRXMAXP6, type R/W, offset 0x164, reset 0x0000 (see page 1068)															
					MAXLOAD										
USBRXMAXP7, type R/W, offset 0x174, reset 0x0000 (see page 1068)															
					MAXLOAD										
USBRXMAXP8, type R/W, offset 0x184, reset 0x0000 (see page 1068)															
					MAXLOAD										
USBRXMAXP9, type R/W, offset 0x194, reset 0x0000 (see page 1068)															
					MAXLOAD										
USBRXMAXP10, type R/W, offset 0x1A4, reset 0x0000 (see page 1068)															
					MAXLOAD										
USBRXMAXP11, type R/W, offset 0x1B4, reset 0x0000 (see page 1068)															
					MAXLOAD										
USBRXMAXP12, type R/W, offset 0x1C4, reset 0x0000 (see page 1068)															
					MAXLOAD										
USBRXMAXP13, type R/W, offset 0x1D4, reset 0x0000 (see page 1068)															
					MAXLOAD										
USBRXMAXP14, type R/W, offset 0x1E4, reset 0x0000 (see page 1068)															
					MAXLOAD										
USBRXMAXP15, type R/W, offset 0x1F4, reset 0x0000 (see page 1068)															
					MAXLOAD										
USBRXCSRL1, type R/W, offset 0x116, reset 0x00 (OTG A / Host Mode) (see page 1070)															
								CLRDT	STALLED	REQPKT	FLUSH	DATAERR / NAKTO	ERROR	FULL	RXRDY
USBRXCSRL2, type R/W, offset 0x126, reset 0x00 (OTG A / Host Mode) (see page 1070)															
								CLRDT	STALLED	REQPKT	FLUSH	DATAERR / NAKTO	ERROR	FULL	RXRDY
USBRXCSRL3, type R/W, offset 0x136, reset 0x00 (OTG A / Host Mode) (see page 1070)															
								CLRDT	STALLED	REQPKT	FLUSH	DATAERR / NAKTO	ERROR	FULL	RXRDY
USBRXCSRL4, type R/W, offset 0x146, reset 0x00 (OTG A / Host Mode) (see page 1070)															
								CLRDT	STALLED	REQPKT	FLUSH	DATAERR / NAKTO	ERROR	FULL	RXRDY

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USBRXCSRL5, type R/W, offset 0x156, reset 0x00 (OTG A / Host Mode) (see page 1070)															
								CLRDT	STALLED	REQPKT	FLUSH	DATAERR / NAKTO	ERROR	FULL	RXRDY
USBRXCSRL6, type R/W, offset 0x166, reset 0x00 (OTG A / Host Mode) (see page 1070)															
								CLRDT	STALLED	REQPKT	FLUSH	DATAERR / NAKTO	ERROR	FULL	RXRDY
USBRXCSRL7, type R/W, offset 0x176, reset 0x00 (OTG A / Host Mode) (see page 1070)															
								CLRDT	STALLED	REQPKT	FLUSH	DATAERR / NAKTO	ERROR	FULL	RXRDY
USBRXCSRL8, type R/W, offset 0x186, reset 0x00 (OTG A / Host Mode) (see page 1070)															
								CLRDT	STALLED	REQPKT	FLUSH	DATAERR / NAKTO	ERROR	FULL	RXRDY
USBRXCSRL9, type R/W, offset 0x196, reset 0x00 (OTG A / Host Mode) (see page 1070)															
								CLRDT	STALLED	REQPKT	FLUSH	DATAERR / NAKTO	ERROR	FULL	RXRDY
USBRXCSRL10, type R/W, offset 0x1A6, reset 0x00 (OTG A / Host Mode) (see page 1070)															
								CLRDT	STALLED	REQPKT	FLUSH	DATAERR / NAKTO	ERROR	FULL	RXRDY
USBRXCSRL11, type R/W, offset 0x1B6, reset 0x00 (OTG A / Host Mode) (see page 1070)															
								CLRDT	STALLED	REQPKT	FLUSH	DATAERR / NAKTO	ERROR	FULL	RXRDY
USBRXCSRL12, type R/W, offset 0x1C6, reset 0x00 (OTG A / Host Mode) (see page 1070)															
								CLRDT	STALLED	REQPKT	FLUSH	DATAERR / NAKTO	ERROR	FULL	RXRDY
USBRXCSRL13, type R/W, offset 0x1D6, reset 0x00 (OTG A / Host Mode) (see page 1070)															
								CLRDT	STALLED	REQPKT	FLUSH	DATAERR / NAKTO	ERROR	FULL	RXRDY
USBRXCSRL14, type R/W, offset 0x1E6, reset 0x00 (OTG A / Host Mode) (see page 1070)															
								CLRDT	STALLED	REQPKT	FLUSH	DATAERR / NAKTO	ERROR	FULL	RXRDY
USBRXCSRL15, type R/W, offset 0x1F6, reset 0x00 (OTG A / Host Mode) (see page 1070)															
								CLRDT	STALLED	REQPKT	FLUSH	DATAERR / NAKTO	ERROR	FULL	RXRDY
USBRXCSRL1, type R/W, offset 0x116, reset 0x00 (OTG B / Device Mode) (see page 1070)															
								CLRDT	STALLED	STALL	FLUSH	DATAERR	OVER	FULL	RXRDY
USBRXCSRL2, type R/W, offset 0x126, reset 0x00 (OTG B / Device Mode) (see page 1070)															
								CLRDT	STALLED	STALL	FLUSH	DATAERR	OVER	FULL	RXRDY
USBRXCSRL3, type R/W, offset 0x136, reset 0x00 (OTG B / Device Mode) (see page 1070)															
								CLRDT	STALLED	STALL	FLUSH	DATAERR	OVER	FULL	RXRDY
USBRXCSRL4, type R/W, offset 0x146, reset 0x00 (OTG B / Device Mode) (see page 1070)															
								CLRDT	STALLED	STALL	FLUSH	DATAERR	OVER	FULL	RXRDY
USBRXCSRL5, type R/W, offset 0x156, reset 0x00 (OTG B / Device Mode) (see page 1070)															
								CLRDT	STALLED	STALL	FLUSH	DATAERR	OVER	FULL	RXRDY
USBRXCSRL6, type R/W, offset 0x166, reset 0x00 (OTG B / Device Mode) (see page 1070)															
								CLRDT	STALLED	STALL	FLUSH	DATAERR	OVER	FULL	RXRDY
USBRXCSRL7, type R/W, offset 0x176, reset 0x00 (OTG B / Device Mode) (see page 1070)															
								CLRDT	STALLED	STALL	FLUSH	DATAERR	OVER	FULL	RXRDY
USBRXCSRL8, type R/W, offset 0x186, reset 0x00 (OTG B / Device Mode) (see page 1070)															
								CLRDT	STALLED	STALL	FLUSH	DATAERR	OVER	FULL	RXRDY
USBRXCSRL9, type R/W, offset 0x196, reset 0x00 (OTG B / Device Mode) (see page 1070)															
								CLRDT	STALLED	STALL	FLUSH	DATAERR	OVER	FULL	RXRDY
USBRXCSRL10, type R/W, offset 0x1A6, reset 0x00 (OTG B / Device Mode) (see page 1070)															
								CLRDT	STALLED	STALL	FLUSH	DATAERR	OVER	FULL	RXRDY
USBRXCSRL11, type R/W, offset 0x1B6, reset 0x00 (OTG B / Device Mode) (see page 1070)															
								CLRDT	STALLED	STALL	FLUSH	DATAERR	OVER	FULL	RXRDY

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USBRXCSRL12, type R/W, offset 0x1C6, reset 0x00 (OTG B / Device Mode) (see page 1070)															
								CLRDT	STALLED	STALL	FLUSH	DATAERR	OVER	FULL	RXRDY
USBRXCSRL13, type R/W, offset 0x1D6, reset 0x00 (OTG B / Device Mode) (see page 1070)															
								CLRDT	STALLED	STALL	FLUSH	DATAERR	OVER	FULL	RXRDY
USBRXCSRL14, type R/W, offset 0x1E6, reset 0x00 (OTG B / Device Mode) (see page 1070)															
								CLRDT	STALLED	STALL	FLUSH	DATAERR	OVER	FULL	RXRDY
USBRXCSRL15, type R/W, offset 0x1F6, reset 0x00 (OTG B / Device Mode) (see page 1070)															
								CLRDT	STALLED	STALL	FLUSH	DATAERR	OVER	FULL	RXRDY
USBRXCSRH1, type R/W, offset 0x117, reset 0x00 (OTG A / Host Mode) (see page 1075)															
								AUTOCL	AUTORQ	DMAEN	PIDERR	DMAMOD	DTWE	DT	
USBRXCSRH2, type R/W, offset 0x127, reset 0x00 (OTG A / Host Mode) (see page 1075)															
								AUTOCL	AUTORQ	DMAEN	PIDERR	DMAMOD	DTWE	DT	
USBRXCSRH3, type R/W, offset 0x137, reset 0x00 (OTG A / Host Mode) (see page 1075)															
								AUTOCL	AUTORQ	DMAEN	PIDERR	DMAMOD	DTWE	DT	
USBRXCSRH4, type R/W, offset 0x147, reset 0x00 (OTG A / Host Mode) (see page 1075)															
								AUTOCL	AUTORQ	DMAEN	PIDERR	DMAMOD	DTWE	DT	
USBRXCSRH5, type R/W, offset 0x157, reset 0x00 (OTG A / Host Mode) (see page 1075)															
								AUTOCL	AUTORQ	DMAEN	PIDERR	DMAMOD	DTWE	DT	
USBRXCSRH6, type R/W, offset 0x167, reset 0x00 (OTG A / Host Mode) (see page 1075)															
								AUTOCL	AUTORQ	DMAEN	PIDERR	DMAMOD	DTWE	DT	
USBRXCSRH7, type R/W, offset 0x177, reset 0x00 (OTG A / Host Mode) (see page 1075)															
								AUTOCL	AUTORQ	DMAEN	PIDERR	DMAMOD	DTWE	DT	
USBRXCSRH8, type R/W, offset 0x187, reset 0x00 (OTG A / Host Mode) (see page 1075)															
								AUTOCL	AUTORQ	DMAEN	PIDERR	DMAMOD	DTWE	DT	
USBRXCSRH9, type R/W, offset 0x197, reset 0x00 (OTG A / Host Mode) (see page 1075)															
								AUTOCL	AUTORQ	DMAEN	PIDERR	DMAMOD	DTWE	DT	
USBRXCSRH10, type R/W, offset 0x1A7, reset 0x00 (OTG A / Host Mode) (see page 1075)															
								AUTOCL	AUTORQ	DMAEN	PIDERR	DMAMOD	DTWE	DT	
USBRXCSRH11, type R/W, offset 0x1B7, reset 0x00 (OTG A / Host Mode) (see page 1075)															
								AUTOCL	AUTORQ	DMAEN	PIDERR	DMAMOD	DTWE	DT	
USBRXCSRH12, type R/W, offset 0x1C7, reset 0x00 (OTG A / Host Mode) (see page 1075)															
								AUTOCL	AUTORQ	DMAEN	PIDERR	DMAMOD	DTWE	DT	
USBRXCSRH13, type R/W, offset 0x1D7, reset 0x00 (OTG A / Host Mode) (see page 1075)															
								AUTOCL	AUTORQ	DMAEN	PIDERR	DMAMOD	DTWE	DT	
USBRXCSRH14, type R/W, offset 0x1E7, reset 0x00 (OTG A / Host Mode) (see page 1075)															
								AUTOCL	AUTORQ	DMAEN	PIDERR	DMAMOD	DTWE	DT	
USBRXCSRH15, type R/W, offset 0x1F7, reset 0x00 (OTG A / Host Mode) (see page 1075)															
								AUTOCL	AUTORQ	DMAEN	PIDERR	DMAMOD	DTWE	DT	
USBRXCSRH1, type R/W, offset 0x117, reset 0x00 (OTG B / Device Mode) (see page 1075)															
								AUTOCL	ISO	DMAEN	DISNYET / PIDERR	DMAMOD			
USBRXCSRH2, type R/W, offset 0x127, reset 0x00 (OTG B / Device Mode) (see page 1075)															
								AUTOCL	ISO	DMAEN	DISNYET / PIDERR	DMAMOD			
USBRXCSRH3, type R/W, offset 0x137, reset 0x00 (OTG B / Device Mode) (see page 1075)															
								AUTOCL	ISO	DMAEN	DISNYET / PIDERR	DMAMOD			
USBRXCSRH4, type R/W, offset 0x147, reset 0x00 (OTG B / Device Mode) (see page 1075)															
								AUTOCL	ISO	DMAEN	DISNYET / PIDERR	DMAMOD			
USBRXCSRH5, type R/W, offset 0x157, reset 0x00 (OTG B / Device Mode) (see page 1075)															
								AUTOCL	ISO	DMAEN	DISNYET / PIDERR	DMAMOD			

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USBRXCSRH6, type R/W, offset 0x167, reset 0x00 (OTG B / Device Mode) (see page 1075)															
								AUTOCL	ISO	DMAEN	DISNYET / PIDERR	DMAMOD			
USBRXCSRH7, type R/W, offset 0x177, reset 0x00 (OTG B / Device Mode) (see page 1075)															
								AUTOCL	ISO	DMAEN	DISNYET / PIDERR	DMAMOD			
USBRXCSRH8, type R/W, offset 0x187, reset 0x00 (OTG B / Device Mode) (see page 1075)															
								AUTOCL	ISO	DMAEN	DISNYET / PIDERR	DMAMOD			
USBRXCSRH9, type R/W, offset 0x197, reset 0x00 (OTG B / Device Mode) (see page 1075)															
								AUTOCL	ISO	DMAEN	DISNYET / PIDERR	DMAMOD			
USBRXCSRH10, type R/W, offset 0x1A7, reset 0x00 (OTG B / Device Mode) (see page 1075)															
								AUTOCL	ISO	DMAEN	DISNYET / PIDERR	DMAMOD			
USBRXCSRH11, type R/W, offset 0x1B7, reset 0x00 (OTG B / Device Mode) (see page 1075)															
								AUTOCL	ISO	DMAEN	DISNYET / PIDERR	DMAMOD			
USBRXCSRH12, type R/W, offset 0x1C7, reset 0x00 (OTG B / Device Mode) (see page 1075)															
								AUTOCL	ISO	DMAEN	DISNYET / PIDERR	DMAMOD			
USBRXCSRH13, type R/W, offset 0x1D7, reset 0x00 (OTG B / Device Mode) (see page 1075)															
								AUTOCL	ISO	DMAEN	DISNYET / PIDERR	DMAMOD			
USBRXCSRH14, type R/W, offset 0x1E7, reset 0x00 (OTG B / Device Mode) (see page 1075)															
								AUTOCL	ISO	DMAEN	DISNYET / PIDERR	DMAMOD			
USBRXCSRH15, type R/W, offset 0x1F7, reset 0x00 (OTG B / Device Mode) (see page 1075)															
								AUTOCL	ISO	DMAEN	DISNYET / PIDERR	DMAMOD			
USBRXCOUNT1, type RO, offset 0x118, reset 0x0000 (see page 1080)															
								COUNT							
USBRXCOUNT2, type RO, offset 0x128, reset 0x0000 (see page 1080)															
								COUNT							
USBRXCOUNT3, type RO, offset 0x138, reset 0x0000 (see page 1080)															
								COUNT							
USBRXCOUNT4, type RO, offset 0x148, reset 0x0000 (see page 1080)															
								COUNT							
USBRXCOUNT5, type RO, offset 0x158, reset 0x0000 (see page 1080)															
								COUNT							
USBRXCOUNT6, type RO, offset 0x168, reset 0x0000 (see page 1080)															
								COUNT							
USBRXCOUNT7, type RO, offset 0x178, reset 0x0000 (see page 1080)															
								COUNT							
USBRXCOUNT8, type RO, offset 0x188, reset 0x0000 (see page 1080)															
								COUNT							
USBRXCOUNT9, type RO, offset 0x198, reset 0x0000 (see page 1080)															
								COUNT							
USBRXCOUNT10, type RO, offset 0x1A8, reset 0x0000 (see page 1080)															
								COUNT							
USBRXCOUNT11, type RO, offset 0x1B8, reset 0x0000 (see page 1080)															
								COUNT							
USBRXCOUNT12, type RO, offset 0x1C8, reset 0x0000 (see page 1080)															
								COUNT							
USBRXCOUNT13, type RO, offset 0x1D8, reset 0x0000 (see page 1080)															
								COUNT							

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USBRXCOUNT14, type RO, offset 0x1E8, reset 0x0000 (see page 1080)															
			COUNT												
USBRXCOUNT15, type RO, offset 0x1F8, reset 0x0000 (see page 1080)															
			COUNT												
USBTXTYPE1, type R/W, offset 0x11A, reset 0x00 (see page 1082)															
								SPEED		PROTO		TEP			
USBTXTYPE2, type R/W, offset 0x12A, reset 0x00 (see page 1082)															
								SPEED		PROTO		TEP			
USBTXTYPE3, type R/W, offset 0x13A, reset 0x00 (see page 1082)															
								SPEED		PROTO		TEP			
USBTXTYPE4, type R/W, offset 0x14A, reset 0x00 (see page 1082)															
								SPEED		PROTO		TEP			
USBTXTYPE5, type R/W, offset 0x15A, reset 0x00 (see page 1082)															
								SPEED		PROTO		TEP			
USBTXTYPE6, type R/W, offset 0x16A, reset 0x00 (see page 1082)															
								SPEED		PROTO		TEP			
USBTXTYPE7, type R/W, offset 0x17A, reset 0x00 (see page 1082)															
								SPEED		PROTO		TEP			
USBTXTYPE8, type R/W, offset 0x18A, reset 0x00 (see page 1082)															
								SPEED		PROTO		TEP			
USBTXTYPE9, type R/W, offset 0x19A, reset 0x00 (see page 1082)															
								SPEED		PROTO		TEP			
USBTXTYPE10, type R/W, offset 0x1AA, reset 0x00 (see page 1082)															
								SPEED		PROTO		TEP			
USBTXTYPE11, type R/W, offset 0x1BA, reset 0x00 (see page 1082)															
								SPEED		PROTO		TEP			
USBTXTYPE12, type R/W, offset 0x1CA, reset 0x00 (see page 1082)															
								SPEED		PROTO		TEP			
USBTXTYPE13, type R/W, offset 0x1DA, reset 0x00 (see page 1082)															
								SPEED		PROTO		TEP			
USBTXTYPE14, type R/W, offset 0x1EA, reset 0x00 (see page 1082)															
								SPEED		PROTO		TEP			
USBTXTYPE15, type R/W, offset 0x1FA, reset 0x00 (see page 1082)															
								SPEED		PROTO		TEP			
USBTXINTERVAL1, type R/W, offset 0x11B, reset 0x00 (see page 1084)															
								TXPOLL / NAKLMT							
USBTXINTERVAL2, type R/W, offset 0x12B, reset 0x00 (see page 1084)															
								TXPOLL / NAKLMT							
USBTXINTERVAL3, type R/W, offset 0x13B, reset 0x00 (see page 1084)															
								TXPOLL / NAKLMT							
USBTXINTERVAL4, type R/W, offset 0x14B, reset 0x00 (see page 1084)															
								TXPOLL / NAKLMT							
USBTXINTERVAL5, type R/W, offset 0x15B, reset 0x00 (see page 1084)															
								TXPOLL / NAKLMT							
USBTXINTERVAL6, type R/W, offset 0x16B, reset 0x00 (see page 1084)															
								TXPOLL / NAKLMT							
USBTXINTERVAL7, type R/W, offset 0x17B, reset 0x00 (see page 1084)															
								TXPOLL / NAKLMT							
USBTXINTERVAL8, type R/W, offset 0x18B, reset 0x00 (see page 1084)															
								TXPOLL / NAKLMT							
USBTXINTERVAL9, type R/W, offset 0x19B, reset 0x00 (see page 1084)															
								TXPOLL / NAKLMT							

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USBTXINTERVAL10, type R/W, offset 0x1AB, reset 0x00 (see page 1084)															
								TXPOLL / NAKLMT							
USBTXINTERVAL11, type R/W, offset 0x1BB, reset 0x00 (see page 1084)															
								TXPOLL / NAKLMT							
USBTXINTERVAL12, type R/W, offset 0x1CB, reset 0x00 (see page 1084)															
								TXPOLL / NAKLMT							
USBTXINTERVAL13, type R/W, offset 0x1DB, reset 0x00 (see page 1084)															
								TXPOLL / NAKLMT							
USBTXINTERVAL14, type R/W, offset 0x1EB, reset 0x00 (see page 1084)															
								TXPOLL / NAKLMT							
USBTXINTERVAL15, type R/W, offset 0x1FB, reset 0x00 (see page 1084)															
								TXPOLL / NAKLMT							
USBRXTYPE1, type R/W, offset 0x11C, reset 0x00 (see page 1086)															
								SPEED		PROTO		TEP			
USBRXTYPE2, type R/W, offset 0x12C, reset 0x00 (see page 1086)															
								SPEED		PROTO		TEP			
USBRXTYPE3, type R/W, offset 0x13C, reset 0x00 (see page 1086)															
								SPEED		PROTO		TEP			
USBRXTYPE4, type R/W, offset 0x14C, reset 0x00 (see page 1086)															
								SPEED		PROTO		TEP			
USBRXTYPE5, type R/W, offset 0x15C, reset 0x00 (see page 1086)															
								SPEED		PROTO		TEP			
USBRXTYPE6, type R/W, offset 0x16C, reset 0x00 (see page 1086)															
								SPEED		PROTO		TEP			
USBRXTYPE7, type R/W, offset 0x17C, reset 0x00 (see page 1086)															
								SPEED		PROTO		TEP			
USBRXTYPE8, type R/W, offset 0x18C, reset 0x00 (see page 1086)															
								SPEED		PROTO		TEP			
USBRXTYPE9, type R/W, offset 0x19C, reset 0x00 (see page 1086)															
								SPEED		PROTO		TEP			
USBRXTYPE10, type R/W, offset 0x1AC, reset 0x00 (see page 1086)															
								SPEED		PROTO		TEP			
USBRXTYPE11, type R/W, offset 0x1BC, reset 0x00 (see page 1086)															
								SPEED		PROTO		TEP			
USBRXTYPE12, type R/W, offset 0x1CC, reset 0x00 (see page 1086)															
								SPEED		PROTO		TEP			
USBRXTYPE13, type R/W, offset 0x1DC, reset 0x00 (see page 1086)															
								SPEED		PROTO		TEP			
USBRXTYPE14, type R/W, offset 0x1EC, reset 0x00 (see page 1086)															
								SPEED		PROTO		TEP			
USBRXTYPE15, type R/W, offset 0x1FC, reset 0x00 (see page 1086)															
								SPEED		PROTO		TEP			
USBRXINTERVAL1, type R/W, offset 0x11D, reset 0x00 (see page 1088)															
								TXPOLL / NAKLMT							
USBRXINTERVAL2, type R/W, offset 0x12D, reset 0x00 (see page 1088)															
								TXPOLL / NAKLMT							
USBRXINTERVAL3, type R/W, offset 0x13D, reset 0x00 (see page 1088)															
								TXPOLL / NAKLMT							
USBRXINTERVAL4, type R/W, offset 0x14D, reset 0x00 (see page 1088)															
								TXPOLL / NAKLMT							
USBRXINTERVAL5, type R/W, offset 0x15D, reset 0x00 (see page 1088)															
								TXPOLL / NAKLMT							

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USBRXINTERVAL6, type R/W, offset 0x16D, reset 0x00 (see page 1088)															
								TXPOLL / NAKLMT							
USBRXINTERVAL7, type R/W, offset 0x17D, reset 0x00 (see page 1088)															
								TXPOLL / NAKLMT							
USBRXINTERVAL8, type R/W, offset 0x18D, reset 0x00 (see page 1088)															
								TXPOLL / NAKLMT							
USBRXINTERVAL9, type R/W, offset 0x19D, reset 0x00 (see page 1088)															
								TXPOLL / NAKLMT							
USBRXINTERVAL10, type R/W, offset 0x1AD, reset 0x00 (see page 1088)															
								TXPOLL / NAKLMT							
USBRXINTERVAL11, type R/W, offset 0x1BD, reset 0x00 (see page 1088)															
								TXPOLL / NAKLMT							
USBRXINTERVAL12, type R/W, offset 0x1CD, reset 0x00 (see page 1088)															
								TXPOLL / NAKLMT							
USBRXINTERVAL13, type R/W, offset 0x1DD, reset 0x00 (see page 1088)															
								TXPOLL / NAKLMT							
USBRXINTERVAL14, type R/W, offset 0x1ED, reset 0x00 (see page 1088)															
								TXPOLL / NAKLMT							
USBRXINTERVAL15, type R/W, offset 0x1FD, reset 0x00 (see page 1088)															
								TXPOLL / NAKLMT							
USBRQPKTCOUNT1, type R/W, offset 0x304, reset 0x0000 (see page 1090)															
								COUNT							
USBRQPKTCOUNT2, type R/W, offset 0x308, reset 0x0000 (see page 1090)															
								COUNT							
USBRQPKTCOUNT3, type R/W, offset 0x30C, reset 0x0000 (see page 1090)															
								COUNT							
USBRQPKTCOUNT4, type R/W, offset 0x310, reset 0x0000 (see page 1090)															
								COUNT							
USBRQPKTCOUNT5, type R/W, offset 0x314, reset 0x0000 (see page 1090)															
								COUNT							
USBRQPKTCOUNT6, type R/W, offset 0x318, reset 0x0000 (see page 1090)															
								COUNT							
USBRQPKTCOUNT7, type R/W, offset 0x31C, reset 0x0000 (see page 1090)															
								COUNT							
USBRQPKTCOUNT8, type R/W, offset 0x320, reset 0x0000 (see page 1090)															
								COUNT							
USBRQPKTCOUNT9, type R/W, offset 0x324, reset 0x0000 (see page 1090)															
								COUNT							
USBRQPKTCOUNT10, type R/W, offset 0x328, reset 0x0000 (see page 1090)															
								COUNT							
USBRQPKTCOUNT11, type R/W, offset 0x32C, reset 0x0000 (see page 1090)															
								COUNT							
USBRQPKTCOUNT12, type R/W, offset 0x330, reset 0x0000 (see page 1090)															
								COUNT							
USBRQPKTCOUNT13, type R/W, offset 0x334, reset 0x0000 (see page 1090)															
								COUNT							
USBRQPKTCOUNT14, type R/W, offset 0x338, reset 0x0000 (see page 1090)															
								COUNT							
USBRQPKTCOUNT15, type R/W, offset 0x33C, reset 0x0000 (see page 1090)															
								COUNT							
USBRXDPKTBUFDIS, type R/W, offset 0x340, reset 0x0000 (see page 1092)															
EP15	EP14	EP13	EP12	EP11	EP10	EP9	EP8	EP7	EP6	EP5	EP4	EP3	EP2	EP1	

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USBTXDPKTBUFDIS, type R/W, offset 0x342, reset 0x0000 (see page 1094)															
EP15	EP14	EP13	EP12	EP11	EP10	EP9	EP8	EP7	EP6	EP5	EP4	EP3	EP2	EP1	
USBEPC, type R/W, offset 0x400, reset 0x0000.0000 (see page 1096)															
						PFLTACT			PFLTAEN	PFLTSEN	PFLTEN		EPENDE	EPEN	
USBEPCRIS, type RO, offset 0x404, reset 0x0000.0000 (see page 1099)															
															PF
USBEPCIM, type R/W, offset 0x408, reset 0x0000.0000 (see page 1100)															
															PF
USBEPCISC, type R/W, offset 0x40C, reset 0x0000.0000 (see page 1101)															
															PF
USBDRRIS, type RO, offset 0x410, reset 0x0000.0000 (see page 1102)															
															RESUME
USBDRIM, type R/W, offset 0x414, reset 0x0000.0000 (see page 1103)															
															RESUME
USBDRISC, type W1C, offset 0x418, reset 0x0000.0000 (see page 1104)															
															RESUME
USBGPCS, type R/W, offset 0x41C, reset 0x0000.0001 (see page 1105)															
														DEVMODOTG	DEVMOD
USBVDC, type R/W, offset 0x430, reset 0x0000.0000 (see page 1106)															
															VBDEN
USBVDCRIS, type RO, offset 0x434, reset 0x0000.0000 (see page 1107)															
															VD
USBVDCIM, type R/W, offset 0x438, reset 0x0000.0000 (see page 1108)															
															VD
USBVDCISC, type R/W, offset 0x43C, reset 0x0000.0000 (see page 1109)															
															VD
USBIDVRIS, type RO, offset 0x444, reset 0x0000.0000 (see page 1110)															
															ID
USBIDVIM, type R/W, offset 0x448, reset 0x0000.0000 (see page 1111)															
															ID
USBIDVISC, type R/W1C, offset 0x44C, reset 0x0000.0000 (see page 1112)															
															ID
USBDMASEL, type R/W, offset 0x450, reset 0x0033.2211 (see page 1113)															
								DMACTX				DMACRX			
DMABTX				DMABRX				DMAATX				DMAARX			

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Analog Comparators Base 0x4003.C000															
ACMIS, type R/W1C, offset 0x000, reset 0x0000.0000 (see page 1122)															
													IN2	IN1	IN0
ACRIS, type RO, offset 0x004, reset 0x0000.0000 (see page 1123)															
													IN2	IN1	IN0
ACINTEN, type R/W, offset 0x008, reset 0x0000.0000 (see page 1124)															
													IN2	IN1	IN0
ACREFCTL, type R/W, offset 0x010, reset 0x0000.0000 (see page 1125)															
						EN	RNG					VREF			
ACSTAT0, type RO, offset 0x020, reset 0x0000.0000 (see page 1126)															
														OVAL	
ACSTAT1, type RO, offset 0x040, reset 0x0000.0000 (see page 1126)															
														OVAL	
ACSTAT2, type RO, offset 0x060, reset 0x0000.0000 (see page 1126)															
														OVAL	
ACCTL0, type R/W, offset 0x024, reset 0x0000.0000 (see page 1127)															
				TOEN	ASRCP			TSLVAL	TSEN		ISLVAL	ISEN		CINV	
ACCTL1, type R/W, offset 0x044, reset 0x0000.0000 (see page 1127)															
				TOEN	ASRCP			TSLVAL	TSEN		ISLVAL	ISEN		CINV	
ACCTL2, type R/W, offset 0x064, reset 0x0000.0000 (see page 1127)															
				TOEN	ASRCP			TSLVAL	TSEN		ISLVAL	ISEN		CINV	
Pulse Width Modulator (PWM) PWM0 base: 0x4002.8000															
PWMCTL, type R/W, offset 0x000, reset 0x0000.0000 (see page 1144)															
												GLOBALSYNC3	GLOBALSYNC2	GLOBALSYNC1	GLOBALSYNC0
PWMSYNC, type R/W, offset 0x004, reset 0x0000.0000 (see page 1146)															
												SYNC3	SYNC2	SYNC1	SYNC0
PWMENABLE, type R/W, offset 0x008, reset 0x0000.0000 (see page 1147)															
								PWM7EN	PWM6EN	PWM5EN	PWM4EN	PWM3EN	PWM2EN	PWM1EN	PWM0EN
PWMINVERT, type R/W, offset 0x00C, reset 0x0000.0000 (see page 1149)															
								PWM7INV	PWM6INV	PWM5INV	PWM4INV	PWM3INV	PWM2INV	PWM1INV	PWM0INV
PWMFAULT, type R/W, offset 0x010, reset 0x0000.0000 (see page 1151)															
								FAULT7	FAULT6	FAULT5	FAULT4	FAULT3	FAULT2	FAULT1	FAULT0
PWMINTEN, type R/W, offset 0x014, reset 0x0000.0000 (see page 1153)															
												INTFAULT3	INTFAULT2	INTFAULT1	INTFAULT0
												INTPWM3	INTPWM2	INTPWM1	INTPWM0

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWMRIS, type RO, offset 0x018, reset 0x0000.0000 (see page 1155)															
												INTFAULT3	INTFAULT2	INTFAULT1	INTFAULT0
												INTPWM3	INTPWM2	INTPWM1	INTPWM0
PWMISC, type R/W1C, offset 0x01C, reset 0x0000.0000 (see page 1158)															
												INTFAULT3	INTFAULT2	INTFAULT1	INTFAULT0
												INTPWM3	INTPWM2	INTPWM1	INTPWM0
PWMSTATUS, type RO, offset 0x020, reset 0x0000.0000 (see page 1161)															
												FAULT3	FAULT2	FAULT1	FAULT0
PWMFAULTVAL, type R/W, offset 0x024, reset 0x0000.0000 (see page 1163)															
								PWM7	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0
PWMENUPD, type R/W, offset 0x028, reset 0x0000.0000 (see page 1165)															
ENUPD7		ENUPD6		ENUPD5		ENUPD4		ENUPD3		ENUPD2		ENUPD1		ENUPD0	
PWM0CTL, type R/W, offset 0x040, reset 0x0000.0000 (see page 1169)															
													LATCH	MINFLTPER	FLTSRC
DBFALLUPD		DBRISEUPD		DBCTLUPD		GENBUPD		GENAUPD		CMPBUPD	CMPAUPD	LOADUPD	DEBUG	MODE	ENABLE
PWM1CTL, type R/W, offset 0x080, reset 0x0000.0000 (see page 1169)															
													LATCH	MINFLTPER	FLTSRC
DBFALLUPD		DBRISEUPD		DBCTLUPD		GENBUPD		GENAUPD		CMPBUPD	CMPAUPD	LOADUPD	DEBUG	MODE	ENABLE
PWM2CTL, type R/W, offset 0x0C0, reset 0x0000.0000 (see page 1169)															
													LATCH	MINFLTPER	FLTSRC
DBFALLUPD		DBRISEUPD		DBCTLUPD		GENBUPD		GENAUPD		CMPBUPD	CMPAUPD	LOADUPD	DEBUG	MODE	ENABLE
PWM3CTL, type R/W, offset 0x100, reset 0x0000.0000 (see page 1169)															
													LATCH	MINFLTPER	FLTSRC
DBFALLUPD		DBRISEUPD		DBCTLUPD		GENBUPD		GENAUPD		CMPBUPD	CMPAUPD	LOADUPD	DEBUG	MODE	ENABLE
PWM0INTEN, type R/W, offset 0x044, reset 0x0000.0000 (see page 1174)															
		TRCMPBD	TRCMPBU	TRCMPAD	TRCMPAU	TRCNTLOAD	TRCNTZERO			INTCMPBD	INTCMPBU	INTCMPAD	INTCMPAU	INTCNTLOAD	INTCNTZERO
PWM1INTEN, type R/W, offset 0x084, reset 0x0000.0000 (see page 1174)															
		TRCMPBD	TRCMPBU	TRCMPAD	TRCMPAU	TRCNTLOAD	TRCNTZERO			INTCMPBD	INTCMPBU	INTCMPAD	INTCMPAU	INTCNTLOAD	INTCNTZERO
PWM2INTEN, type R/W, offset 0x0C4, reset 0x0000.0000 (see page 1174)															
		TRCMPBD	TRCMPBU	TRCMPAD	TRCMPAU	TRCNTLOAD	TRCNTZERO			INTCMPBD	INTCMPBU	INTCMPAD	INTCMPAU	INTCNTLOAD	INTCNTZERO
PWM3INTEN, type R/W, offset 0x104, reset 0x0000.0000 (see page 1174)															
		TRCMPBD	TRCMPBU	TRCMPAD	TRCMPAU	TRCNTLOAD	TRCNTZERO			INTCMPBD	INTCMPBU	INTCMPAD	INTCMPAU	INTCNTLOAD	INTCNTZERO
PWM0RIS, type RO, offset 0x048, reset 0x0000.0000 (see page 1177)															
										INTCMPBD	INTCMPBU	INTCMPAD	INTCMPAU	INTCNTLOAD	INTCNTZERO
PWM1RIS, type RO, offset 0x088, reset 0x0000.0000 (see page 1177)															
										INTCMPBD	INTCMPBU	INTCMPAD	INTCMPAU	INTCNTLOAD	INTCNTZERO
PWM2RIS, type RO, offset 0x0C8, reset 0x0000.0000 (see page 1177)															
										INTCMPBD	INTCMPBU	INTCMPAD	INTCMPAU	INTCNTLOAD	INTCNTZERO
PWM3RIS, type RO, offset 0x108, reset 0x0000.0000 (see page 1177)															
										INTCMPBD	INTCMPBU	INTCMPAD	INTCMPAU	INTCNTLOAD	INTCNTZERO

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWM0ISC, type R/W1C, offset 0x04C, reset 0x0000.0000 (see page 1179)															
										INTCMPBD	INTCMPBU	INTCMPAD	INTCMPAU	INTCNTLOAD	INTCNTZERO
PWM1ISC, type R/W1C, offset 0x08C, reset 0x0000.0000 (see page 1179)															
										INTCMPBD	INTCMPBU	INTCMPAD	INTCMPAU	INTCNTLOAD	INTCNTZERO
PWM2ISC, type R/W1C, offset 0x0CC, reset 0x0000.0000 (see page 1179)															
										INTCMPBD	INTCMPBU	INTCMPAD	INTCMPAU	INTCNTLOAD	INTCNTZERO
PWM3ISC, type R/W1C, offset 0x10C, reset 0x0000.0000 (see page 1179)															
										INTCMPBD	INTCMPBU	INTCMPAD	INTCMPAU	INTCNTLOAD	INTCNTZERO
PWM0LOAD, type R/W, offset 0x050, reset 0x0000.0000 (see page 1181)															
LOAD															
PWM1LOAD, type R/W, offset 0x090, reset 0x0000.0000 (see page 1181)															
LOAD															
PWM2LOAD, type R/W, offset 0x0D0, reset 0x0000.0000 (see page 1181)															
LOAD															
PWM3LOAD, type R/W, offset 0x110, reset 0x0000.0000 (see page 1181)															
LOAD															
PWM0COUNT, type RO, offset 0x054, reset 0x0000.0000 (see page 1182)															
COUNT															
PWM1COUNT, type RO, offset 0x094, reset 0x0000.0000 (see page 1182)															
COUNT															
PWM2COUNT, type RO, offset 0x0D4, reset 0x0000.0000 (see page 1182)															
COUNT															
PWM3COUNT, type RO, offset 0x114, reset 0x0000.0000 (see page 1182)															
COUNT															
PWM0CMPA, type R/W, offset 0x058, reset 0x0000.0000 (see page 1183)															
COMPA															
PWM1CMPA, type R/W, offset 0x098, reset 0x0000.0000 (see page 1183)															
COMPA															
PWM2CMPA, type R/W, offset 0x0D8, reset 0x0000.0000 (see page 1183)															
COMPA															
PWM3CMPA, type R/W, offset 0x118, reset 0x0000.0000 (see page 1183)															
COMPA															
PWM0CMPB, type R/W, offset 0x05C, reset 0x0000.0000 (see page 1184)															
COMPB															

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWM1CMPB, type R/W, offset 0x09C, reset 0x0000.0000 (see page 1184)															
COMPB															
PWM2CMPB, type R/W, offset 0x0DC, reset 0x0000.0000 (see page 1184)															
COMPB															
PWM3CMPB, type R/W, offset 0x11C, reset 0x0000.0000 (see page 1184)															
COMPB															
PWM0GENA, type R/W, offset 0x060, reset 0x0000.0000 (see page 1185)															
				ACTCMPBD		ACTCMPBU		ACTCMPAD		ACTCMPAU		ACTLOAD		ACTZERO	
PWM1GENA, type R/W, offset 0x0A0, reset 0x0000.0000 (see page 1185)															
				ACTCMPBD		ACTCMPBU		ACTCMPAD		ACTCMPAU		ACTLOAD		ACTZERO	
PWM2GENA, type R/W, offset 0x0E0, reset 0x0000.0000 (see page 1185)															
				ACTCMPBD		ACTCMPBU		ACTCMPAD		ACTCMPAU		ACTLOAD		ACTZERO	
PWM3GENA, type R/W, offset 0x120, reset 0x0000.0000 (see page 1185)															
				ACTCMPBD		ACTCMPBU		ACTCMPAD		ACTCMPAU		ACTLOAD		ACTZERO	
PWM0GENB, type R/W, offset 0x064, reset 0x0000.0000 (see page 1188)															
				ACTCMPBD		ACTCMPBU		ACTCMPAD		ACTCMPAU		ACTLOAD		ACTZERO	
PWM1GENB, type R/W, offset 0x0A4, reset 0x0000.0000 (see page 1188)															
				ACTCMPBD		ACTCMPBU		ACTCMPAD		ACTCMPAU		ACTLOAD		ACTZERO	
PWM2GENB, type R/W, offset 0x0E4, reset 0x0000.0000 (see page 1188)															
				ACTCMPBD		ACTCMPBU		ACTCMPAD		ACTCMPAU		ACTLOAD		ACTZERO	
PWM3GENB, type R/W, offset 0x124, reset 0x0000.0000 (see page 1188)															
				ACTCMPBD		ACTCMPBU		ACTCMPAD		ACTCMPAU		ACTLOAD		ACTZERO	
PWM0DBCTL, type R/W, offset 0x068, reset 0x0000.0000 (see page 1191)															
															ENABLE
PWM1DBCTL, type R/W, offset 0x0A8, reset 0x0000.0000 (see page 1191)															
															ENABLE
PWM2DBCTL, type R/W, offset 0x0E8, reset 0x0000.0000 (see page 1191)															
															ENABLE
PWM3DBCTL, type R/W, offset 0x128, reset 0x0000.0000 (see page 1191)															
															ENABLE
PWM0DBRISE, type R/W, offset 0x06C, reset 0x0000.0000 (see page 1192)															
				RISEDELAY											
PWM1DBRISE, type R/W, offset 0x0AC, reset 0x0000.0000 (see page 1192)															
				RISEDELAY											

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWM2DBRISE, type R/W, offset 0x0EC, reset 0x0000.0000 (see page 1192)															
				RISEDELAY											
PWM3DBRISE, type R/W, offset 0x12C, reset 0x0000.0000 (see page 1192)															
				RISEDELAY											
PWM0DBFALL, type R/W, offset 0x070, reset 0x0000.0000 (see page 1193)															
				FALLDELAY											
PWM1DBFALL, type R/W, offset 0x0B0, reset 0x0000.0000 (see page 1193)															
				FALLDELAY											
PWM2DBFALL, type R/W, offset 0x0F0, reset 0x0000.0000 (see page 1193)															
				FALLDELAY											
PWM3DBFALL, type R/W, offset 0x130, reset 0x0000.0000 (see page 1193)															
				FALLDELAY											
PWM0FLTSRC0, type R/W, offset 0x074, reset 0x0000.0000 (see page 1194)															
												FAULT3	FAULT2	FAULT1	FAULT0
PWM1FLTSRC0, type R/W, offset 0x0B4, reset 0x0000.0000 (see page 1194)															
												FAULT3	FAULT2	FAULT1	FAULT0
PWM2FLTSRC0, type R/W, offset 0x0F4, reset 0x0000.0000 (see page 1194)															
												FAULT3	FAULT2	FAULT1	FAULT0
PWM3FLTSRC0, type R/W, offset 0x134, reset 0x0000.0000 (see page 1194)															
												FAULT3	FAULT2	FAULT1	FAULT0
PWM0FLTSRC1, type R/W, offset 0x078, reset 0x0000.0000 (see page 1196)															
								DCMP7	DCMP6	DCMP5	DCMP4	DCMP3	DCMP2	DCMP1	DCMP0
PWM1FLTSRC1, type R/W, offset 0x0B8, reset 0x0000.0000 (see page 1196)															
								DCMP7	DCMP6	DCMP5	DCMP4	DCMP3	DCMP2	DCMP1	DCMP0
PWM2FLTSRC1, type R/W, offset 0x0F8, reset 0x0000.0000 (see page 1196)															
								DCMP7	DCMP6	DCMP5	DCMP4	DCMP3	DCMP2	DCMP1	DCMP0
PWM3FLTSRC1, type R/W, offset 0x138, reset 0x0000.0000 (see page 1196)															
								DCMP7	DCMP6	DCMP5	DCMP4	DCMP3	DCMP2	DCMP1	DCMP0
PWM0MINFLTPER, type R/W, offset 0x07C, reset 0x0000.0000 (see page 1199)															
MFP															
PWM1MINFLTPER, type R/W, offset 0x0BC, reset 0x0000.0000 (see page 1199)															
MFP															
PWM2MINFLTPER, type R/W, offset 0x0FC, reset 0x0000.0000 (see page 1199)															
MFP															

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWM3MINFLTPER, type R/W, offset 0x13C, reset 0x0000.0000 (see page 1199)															
MFP															
PWM0FLTSEN, type R/W, offset 0x800, reset 0x0000.0000 (see page 1200)															
												FAULT3	FAULT2	FAULT1	FAULT0
PWM1FLTSEN, type R/W, offset 0x880, reset 0x0000.0000 (see page 1200)															
												FAULT3	FAULT2	FAULT1	FAULT0
PWM2FLTSEN, type R/W, offset 0x900, reset 0x0000.0000 (see page 1200)															
												FAULT3	FAULT2	FAULT1	FAULT0
PWM3FLTSEN, type R/W, offset 0x980, reset 0x0000.0000 (see page 1200)															
												FAULT3	FAULT2	FAULT1	FAULT0
PWM0FLTSTAT0, type -, offset 0x804, reset 0x0000.0000 (see page 1201)															
												FAULT3	FAULT2	FAULT1	FAULT0
PWM1FLTSTAT0, type -, offset 0x884, reset 0x0000.0000 (see page 1201)															
												FAULT3	FAULT2	FAULT1	FAULT0
PWM2FLTSTAT0, type -, offset 0x904, reset 0x0000.0000 (see page 1201)															
												FAULT3	FAULT2	FAULT1	FAULT0
PWM3FLTSTAT0, type -, offset 0x984, reset 0x0000.0000 (see page 1201)															
												FAULT3	FAULT2	FAULT1	FAULT0
PWM0FLTSTAT1, type -, offset 0x808, reset 0x0000.0000 (see page 1203)															
								DCMP7	DCMP6	DCMP5	DCMP4	DCMP3	DCMP2	DCMP1	DCMP0
PWM1FLTSTAT1, type -, offset 0x888, reset 0x0000.0000 (see page 1203)															
								DCMP7	DCMP6	DCMP5	DCMP4	DCMP3	DCMP2	DCMP1	DCMP0
PWM2FLTSTAT1, type -, offset 0x908, reset 0x0000.0000 (see page 1203)															
								DCMP7	DCMP6	DCMP5	DCMP4	DCMP3	DCMP2	DCMP1	DCMP0
PWM3FLTSTAT1, type -, offset 0x988, reset 0x0000.0000 (see page 1203)															
								DCMP7	DCMP6	DCMP5	DCMP4	DCMP3	DCMP2	DCMP1	DCMP0
Quadrature Encoder Interface (QEI) QEI0 base: 0x4002.C000 QEI1 base: 0x4002.D000															
QEICTL, type R/W, offset 0x000, reset 0x0000.0000 (see page 1213)															
												FILTCNT			
		FILTEN	STALLEN	INVI	INVB	INVA	VELDIV			VELEN	RESMODE	CAPMODE	SIGMODE	SWAP	ENABLE
QEISTAT, type RO, offset 0x004, reset 0x0000.0000 (see page 1216)															
														DIRECTION	ERROR
QEIPOS, type R/W, offset 0x008, reset 0x0000.0000 (see page 1217)															
POSITION															
POSITION															

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QEIMAXPOS, type R/W, offset 0x00C, reset 0x0000.0000 (see page 1218)															
MAXPOS															
MAXPOS															
QEILOAD, type R/W, offset 0x010, reset 0x0000.0000 (see page 1219)															
LOAD															
LOAD															
QEITIME, type RO, offset 0x014, reset 0x0000.0000 (see page 1220)															
TIME															
TIME															
QEICOUNT, type RO, offset 0x018, reset 0x0000.0000 (see page 1221)															
COUNT															
COUNT															
QEISPEED, type RO, offset 0x01C, reset 0x0000.0000 (see page 1222)															
SPEED															
SPEED															
QEIINTEN, type R/W, offset 0x020, reset 0x0000.0000 (see page 1223)															
												INTERROR	INTDIR	INTTIMER	INTINDEX
QEIRIS, type RO, offset 0x024, reset 0x0000.0000 (see page 1225)															
												INTERROR	INTDIR	INTTIMER	INTINDEX
QEIISC, type R/W1C, offset 0x028, reset 0x0000.0000 (see page 1227)															
												INTERROR	INTDIR	INTTIMER	INTINDEX