

12 Analog-to-Digital Converter (ADC)

An analog-to-digital converter (ADC) is a peripheral that converts a continuous analog voltage to a discrete digital number. Two identical converter modules are included, which share 16 input channels.

The Stellaris® ADC module features 10-bit conversion resolution and supports 16 input channels, plus an internal temperature sensor. Each ADC module contains four programmable sequencers allowing the sampling of multiple analog input sources without controller intervention. Each sample sequencer provides flexible programming with fully configurable input source, trigger events, interrupt generation, and sequencer priority. A digital comparator function is included which allows the conversion value to be diverted to a digital comparator module. Each ADC module provides eight digital comparators. Each digital comparator evaluates the ADC conversion value against its two user-defined values to determine the operational range of the signal. The trigger source for ADC0 and ADC1 may be independent or the two ADC modules may operate from the same trigger source and operate on the same or different inputs. A phase shifter can delay the start of sampling by a specified phase angle. When using both ADC modules, it is possible to configure the converters to start the conversions coincidentally or within a relative phase from each other, see “Sample Phase Control” on page 609.

The Stellaris LM3S9B95 microcontroller provides two ADC modules with each having the following features:

- 16 shared analog input channels
- Single-ended and differential-input configurations
- On-chip internal temperature sensor
- Maximum sample rate of one million samples/second
- Optional phase shift in sample time programmable from 22.5° to 337.5°
- Four programmable sample conversion sequencers from one to eight entries long, with corresponding conversion result FIFOs
- Flexible trigger control
 - Controller (software)
 - Timers
 - Analog Comparators
 - PWM
 - GPIO
- Hardware averaging of up to 64 samples
- Digital comparison unit providing eight digital comparators
- Converter uses an internal 3-V reference or an external reference
- Power and ground for the analog circuitry is separate from the digital power and ground

- Efficient transfers using Micro Direct Memory Access Controller (μ DMA)
 - Dedicated channel for each sample sequencer
 - ADC module uses burst requests for DMA

12.1 Block Diagram

The Stellaris microcontroller contains two identical Analog-to-Digital Converter modules. These two modules, ADC0 and ADC1, share the same 16 analog input channels. Each ADC module operates independently and can therefore execute different sample sequences, sample any of the analog input channels at any time, and generate different interrupts and triggers. Figure 12-1 on page 604 shows how the two modules are connected to analog inputs and the system bus.

Figure 12-1. Implementation of Two ADC Blocks

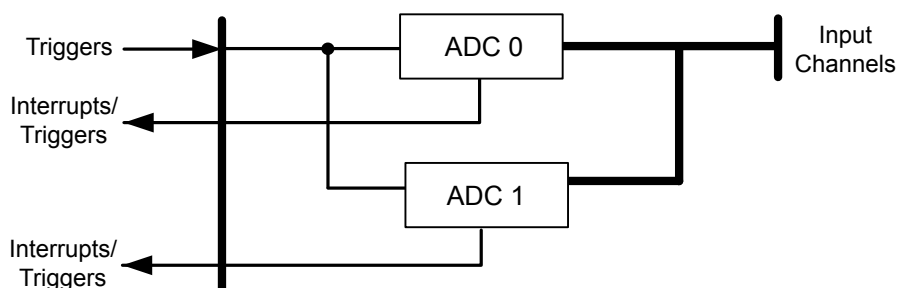
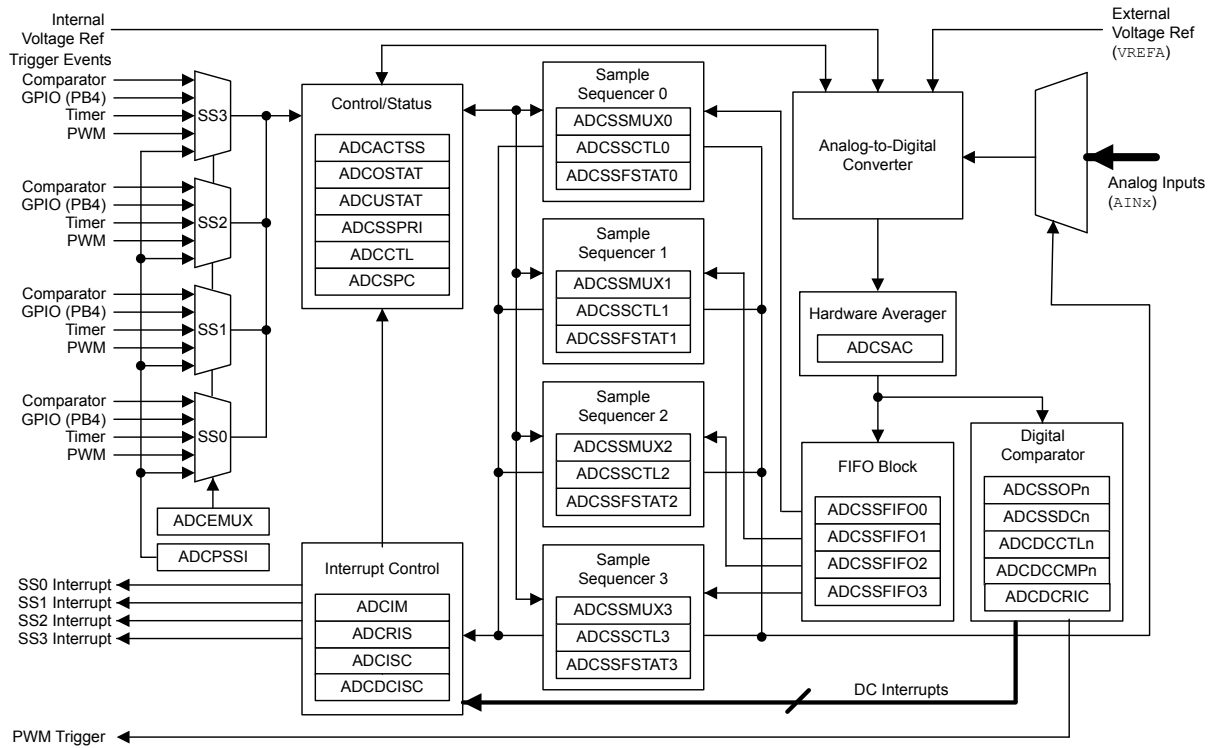


Figure 12-2 on page 605 provides details on the internal configuration of the ADC controls and data registers.

Figure 12-2. ADC Module Block Diagram



12.2 Signal Description

The following table lists the external signals of the ADC module and describes the function of each. The ADC signals are analog functions for some GPIO signals. The column in the table below titled "Pin Mux/Pin Assignment" lists the GPIO pin placement for the ADC signals. The AIN_x and $VREF_A$ analog signals are not 5-V tolerant and go through an isolation circuit before reaching their circuitry. These signals are configured by clearing the corresponding DEN bit in the **GPIO Digital Enable (GPIO DEN)** register and setting the corresponding $AMSEL$ bit in the **GPIO Analog Mode Select (GPIO AMSEL)** register. For more information on configuring GPIOs, see "General-Purpose Input/Outputs (GPIOs)" on page 402.

Table 12-1. ADC Signals (100LQFP)

Pin Name	Pin Number	Pin Mux / Pin Assignment	Pin Type	Buffer Type ^a	Description
AIN0	1	PE7	I	Analog	Analog-to-digital converter input 0.
AIN1	2	PE6	I	Analog	Analog-to-digital converter input 1.
AIN2	5	PE5	I	Analog	Analog-to-digital converter input 2.
AIN3	6	PE4	I	Analog	Analog-to-digital converter input 3.
AIN4	100	PD7	I	Analog	Analog-to-digital converter input 4.
AIN5	99	PD6	I	Analog	Analog-to-digital converter input 5.
AIN6	98	PD5	I	Analog	Analog-to-digital converter input 6.
AIN7	97	PD4	I	Analog	Analog-to-digital converter input 7.
AIN8	96	PE3	I	Analog	Analog-to-digital converter input 8.
AIN9	95	PE2	I	Analog	Analog-to-digital converter input 9.

Table 12-1. ADC Signals (100LQFP) (continued)

Pin Name	Pin Number	Pin Mux / Pin Assignment	Pin Type	Buffer Type ^a	Description
AIN10	92	PB4	I	Analog	Analog-to-digital converter input 10.
AIN11	91	PB5	I	Analog	Analog-to-digital converter input 11.
AIN12	13	PD3	I	Analog	Analog-to-digital converter input 12.
AIN13	12	PD2	I	Analog	Analog-to-digital converter input 13.
AIN14	11	PD1	I	Analog	Analog-to-digital converter input 14.
AIN15	10	PD0	I	Analog	Analog-to-digital converter input 15.
VREFA	90	PB6	I	Analog	This input provides a reference voltage used to specify the input voltage at which the ADC converts to a maximum value. In other words, the voltage that is applied to VREFA is the voltage with which an AIN _n signal is converted to 1023. The VREFA input is limited to the range specified in Table 26-23 on page 1326 .

a. The TTL designation indicates the pin has TTL-compatible voltage levels.

Table 12-2. ADC Signals (108BGA)

Pin Name	Pin Number	Pin Mux / Pin Assignment	Pin Type	Buffer Type ^a	Description
AIN0	B1	PE7	I	Analog	Analog-to-digital converter input 0.
AIN1	A1	PE6	I	Analog	Analog-to-digital converter input 1.
AIN2	B3	PE5	I	Analog	Analog-to-digital converter input 2.
AIN3	B2	PE4	I	Analog	Analog-to-digital converter input 3.
AIN4	A2	PD7	I	Analog	Analog-to-digital converter input 4.
AIN5	A3	PD6	I	Analog	Analog-to-digital converter input 5.
AIN6	C6	PD5	I	Analog	Analog-to-digital converter input 6.
AIN7	B5	PD4	I	Analog	Analog-to-digital converter input 7.
AIN8	B4	PE3	I	Analog	Analog-to-digital converter input 8.
AIN9	A4	PE2	I	Analog	Analog-to-digital converter input 9.
AIN10	A6	PB4	I	Analog	Analog-to-digital converter input 10.
AIN11	B7	PB5	I	Analog	Analog-to-digital converter input 11.
AIN12	H1	PD3	I	Analog	Analog-to-digital converter input 12.
AIN13	H2	PD2	I	Analog	Analog-to-digital converter input 13.
AIN14	G2	PD1	I	Analog	Analog-to-digital converter input 14.
AIN15	G1	PD0	I	Analog	Analog-to-digital converter input 15.
VREFA	A7	PB6	I	Analog	This input provides a reference voltage used to specify the input voltage at which the ADC converts to a maximum value. In other words, the voltage that is applied to VREFA is the voltage with which an AIN _n signal is converted to 1023. The VREFA input is limited to the range specified in Table 26-23 on page 1326 .

a. The TTL designation indicates the pin has TTL-compatible voltage levels.

12.3 Functional Description

The Stellaris ADC collects sample data by using a programmable sequence-based approach instead of the traditional single or double-sampling approaches found on many ADC modules. Each *sample sequence* is a fully programmed series of consecutive (back-to-back) samples, allowing the ADC to collect data from multiple input sources without having to be re-configured or serviced by the processor. The programming of each sample in the sample sequence includes parameters such as the input source and mode (differential versus single-ended input), interrupt generation on sample completion, and the indicator for the last sample in the sequence. In addition, the μ DMA can be used to more efficiently move data from the sample sequencers without CPU intervention.

12.3.1 Sample Sequencers

The sampling control and data capture is handled by the sample sequencers. All of the sequencers are identical in implementation except for the number of samples that can be captured and the depth of the FIFO. Table 12-3 on page 607 shows the maximum number of samples that each sequencer can capture and its corresponding FIFO depth. Each sample that is captured is stored in the FIFO. In this implementation, each FIFO entry is a 32-bit word, with the lower 10 bits containing the conversion result.

Table 12-3. Samples and FIFO Depth of Sequencers

Sequencer	Number of Samples	Depth of FIFO
SS3	1	1
SS2	4	4
SS1	4	4
SS0	8	8

For a given sample sequence, each sample is defined by bit fields in the **ADC Sample Sequence Input Multiplexer Select (ADCSSMUXn)** and **ADC Sample Sequence Control (ADCSSCTLn)** registers, where "n" corresponds to the sequence number. The **ADCSSMUXn** fields select the input pin, while the **ADCSSCTLn** fields contain the sample control bits corresponding to parameters such as temperature sensor selection, interrupt enable, end of sequence, and differential input mode. Sample sequencers are enabled by setting the respective **ASENn** bit in the **ADC Active Sample Sequencer (ADCACTSS)** register and should be configured before being enabled. Sampling is then initiated by setting the **SSn** bit in the **ADC Processor Sample Sequence Initiate (ADCPSSI)** register. In addition, sample sequences may be initiated on multiple ADC modules simultaneously using the **GSYNC** and **SYNCWAIT** bits in the **ADCPSSI** register during the configuration of each ADC module. For more information on using these bits, refer to page 646.

When configuring a sample sequence, multiple uses of the same input pin within the same sequence are allowed. In the **ADCSSCTLn** register, the **IEN** bits can be set for any combination of samples, allowing interrupts to be generated after every sample in the sequence if necessary. Also, the **END** bit can be set at any point within a sample sequence. For example, if Sequencer 0 is used, the **END** bit can be set in the nibble associated with the fifth sample, allowing Sequencer 0 to complete execution of the sample sequence after the fifth sample.

After a sample sequence completes execution, the result data can be retrieved from the **ADC Sample Sequence Result FIFO (ADCSSFIFOn)** registers. The FIFOs are simple circular buffers that read a single address to "pop" result data. For software debug purposes, the positions of the FIFO head and tail pointers are visible in the **ADC Sample Sequence FIFO Status (ADCSSFSTATn)** registers along with **FULL** and **EMPTY** status flags. If a write is attempted when the FIFO is full, the write does not occur and an overflow condition is indicated. Overflow and underflow conditions are monitored using the **ADCOSTAT** and **ADCUSTAT** registers.

12.3.2 Module Control

Outside of the sample sequencers, the remainder of the control logic is responsible for tasks such as:

- Interrupt generation
- DMA operation
- Sequence prioritization
- Trigger configuration
- Comparator configuration
- External voltage reference
- Sample phase control

Most of the ADC control logic runs at the ADC clock rate of 16 MHz. The internal ADC divider is configured for 16-MHz operation automatically by hardware when the system XTAL is selected with the PLL.

12.3.2.1 Interrupts

The register configurations of the sample sequencers and digital comparators dictate which events generate raw interrupts, but do not have control over whether the interrupt is actually sent to the interrupt controller. The ADC module's interrupt signals are controlled by the state of the MASK bits in the **ADC Interrupt Mask (ADCIM)** register. Interrupt status can be viewed at two locations: the **ADC Raw Interrupt Status (ADC RIS)** register, which shows the raw status of the various interrupt signals; and the **ADC Interrupt Status and Clear (ADCISC)** register, which shows active interrupts that are enabled by the ADCIM register. Sequencer interrupts are cleared by writing a 1 to the corresponding IN bit in ADCISC. Digital comparator interrupts are cleared by writing a 1 to the **ADC Digital Comparator Interrupt Status and Clear (ADCDCISC)** register.

12.3.2.2 DMA Operation

DMA may be used to increase efficiency by allowing each sample sequencer to operate independently and transfer data without processor intervention or reconfiguration. The ADC module provides a request signal from each sample sequencer to the associated dedicated channel of the μ DMA controller. The ADC does not support single transfer requests. A burst transfer request is asserted when the interrupt bit for the sample sequence is set (IE bit in the **ADCSSCTLn** register is set).

The arbitration size of the μ DMA transfer must be a power of 2, and the associated IE bits in the **ADCSSCTLn** register must be set. For example, if the μ DMA channel of SS0 has an arbitration size of four, the IE3 bit (4th sample) and the IE7 bit (8th sample) must be set. Thus the μ DMA request occurs every time 4 samples have been acquired. No other special steps are needed to enable the ADC module for μ DMA operation.

Refer to the “Micro Direct Memory Access (μ DMA)” on page 344 for more details about programming the μ DMA controller.

12.3.2.3 Prioritization

When sampling events (triggers) happen concurrently, they are prioritized for processing by the values in the **ADC Sample Sequencer Priority (ADCSSPRI)** register. Valid priority values are in the range of 0-3, with 0 being the highest priority and 3 being the lowest. Multiple active sample

sequencer units with the same priority do not provide consistent results, so software must ensure that all active sample sequencer units have a unique priority value.

12.3.2.4 Sampling Events

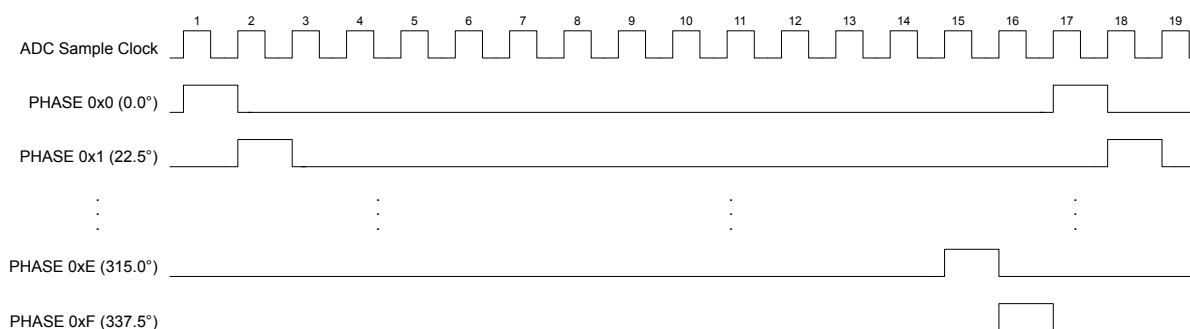
Sample triggering for each sample sequencer is defined in the **ADC Event Multiplexer Select (ADCEMUX)** register. Trigger sources include processor (default), analog comparators, an external signal on GPIO $PB4$, a GP Timer, a PWM generator, and continuous sampling. The processor triggers sampling by setting the SS_x bits in the **ADC Processor Sample Sequence Initiate (ADCPSSI)** register.

Care must be taken when using the continuous sampling trigger. If a sequencer's priority is too high, it is possible to starve other lower priority sequencers. Generally, a sample sequencer using continuous sampling should be set to the lowest priority. Continuous sampling can be used with a digital comparator to cause an interrupt when a particular voltage is seen on an input.

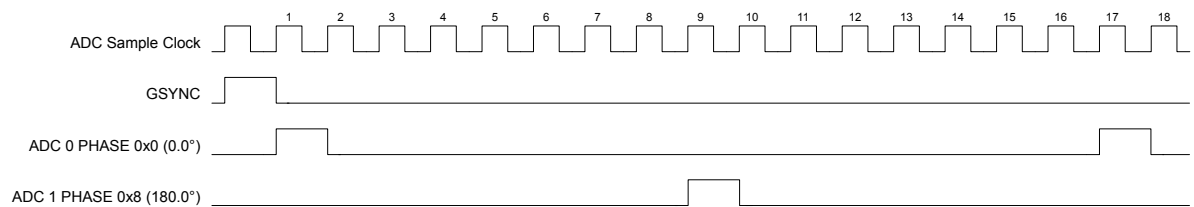
12.3.2.5 Sample Phase Control

The trigger source for ADC0 and ADC1 may be independent or the two ADC modules may operate from the same trigger source and operate on the same or different inputs. If the converters are running at the same sample rate, they may be configured to start the conversions coincidentally or with one of 15 different discrete phases relative to each other. The sample time can be delayed from the standard sampling time in 22.5° increments up to 337.5° using the **ADC Sample Phase Control (ADCSPC)** register. Figure 12-3 on page 609 shows an example of various phase relationships at a 1 Msps rate.

Figure 12-3. ADC Sample Phases

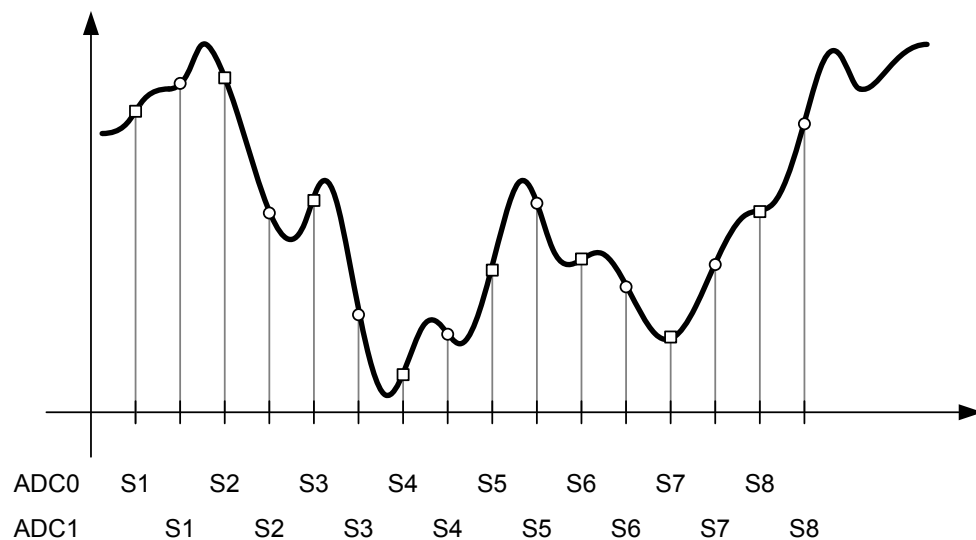


This feature can be used to double the sampling rate of an input. Both ADC module 0 and ADC module 1 can be programmed to sample the same input. ADC module 0 could sample at the standard position (the $PHASE$ field in the **ADCSPC** register is 0x0). ADC module 1 can be configured to sample at 180 ($PHASE = 0x8$). The two modules can be synchronized using the $GSYNC$ and $SYNCWAIT$ bits in the **ADC Processor Sample Sequence Initiate (ADCPSSI)** register. Software could then combine the results from the two modules to create a sample rate of two million samples/second at 16 MHz as shown in Figure 12-4 on page 610.

Figure 12-4. Doubling the ADC Sample Rate

Using the **ADCSPC** register, ADC0 and ADC1 may provide a number of interesting applications:

- Coincident sampling of different signals. The sample sequence steps run coincidentally in both converters.
 - ADC Module 0, **ADCSPC** = 0x0, sampling **AIN0**
 - ADC Module 1, **ADCSPC** = 0x0, sampling **AIN1**
- Skewed sampling of the same signal. The sample sequence steps are 1/2 of an ADC clock (500 μ s for a 1Ms/s ADC) out of phase with each other. This configuration doubles the conversion bandwidth of a single input when software combines the results as shown in Figure 12-5 on page 610.
 - ADC Module 0, **ADCSPC** = 0x0, sampling **AIN0**
 - ADC Module 1, **ADCSPC** = 0x8, sampling **AIN0**

Figure 12-5. Skewed Sampling

12.3.3 Hardware Sample Averaging Circuit

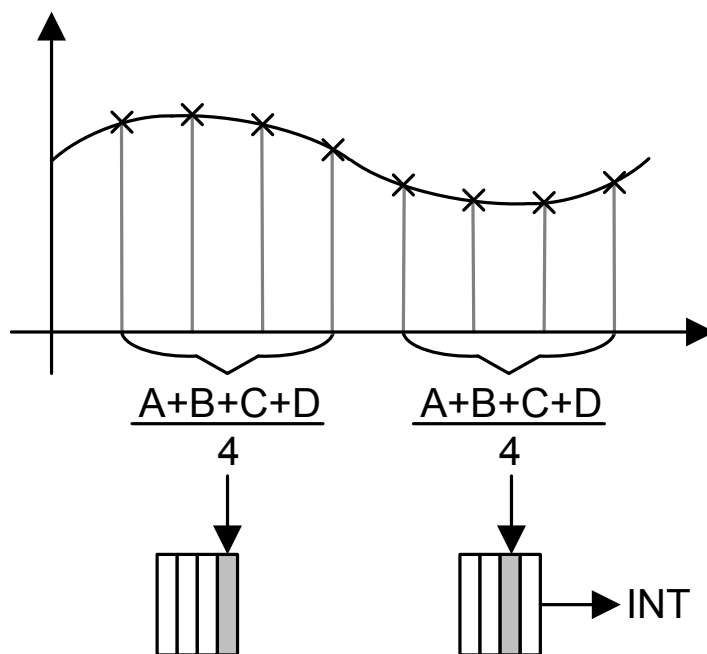
Higher precision results can be generated using the hardware averaging circuit, however, the improved results are at the cost of throughput. Up to 64 samples can be accumulated and averaged to form a single data entry in the sequencer FIFO. Throughput is decreased proportionally to the

number of samples in the averaging calculation. For example, if the averaging circuit is configured to average 16 samples, the throughput is decreased by a factor of 16.

By default the averaging circuit is off, and all data from the converter passes through to the sequencer FIFO. The averaging hardware is controlled by the **ADC Sample Averaging Control (ADCSAC)** register (see page 648). A single averaging circuit has been implemented, thus all input channels receive the same amount of averaging whether they are single-ended or differential.

Figure 12-6 shows an example in which the **ADCSAC** register is set to 0x2 for 4x hardware oversampling and the **IE1** bit is set for the sample sequence, resulting in an interrupt after the second averaged value is stored in the FIFO.

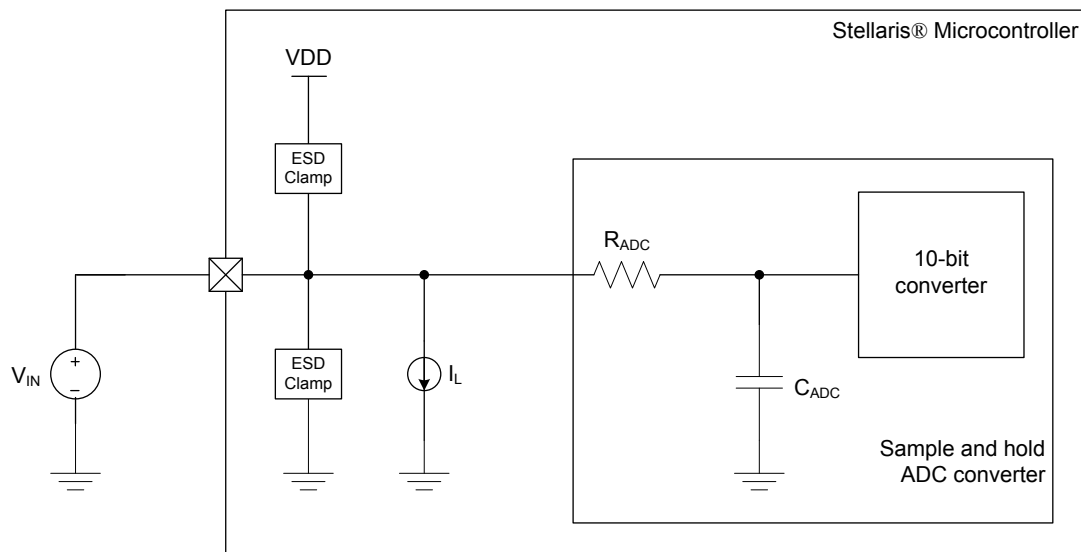
Figure 12-6. Sample Averaging Example



12.3.4 Analog-to-Digital Converter

The Analog-to-Digital Converter (ADC) module uses a Successive Approximation Register (SAR) architecture to deliver a 10-bit, low-power, high-precision conversion value. The successive-approximation algorithm uses a current mode D/A converter to achieve lower settling time, resulting in higher conversion speeds for the A/D converter. In addition, built-in sample-and-hold circuitry with offset-calibration circuitry improves conversion accuracy. The ADC must be run from the PLL or a 16-MHz clock source. Figure 12-7 shows the ADC input equivalency diagram; for parameter values, see “Analog-to-Digital Converter (ADC)” on page 1325.

Figure 12-7. ADC Input Equivalency Diagram

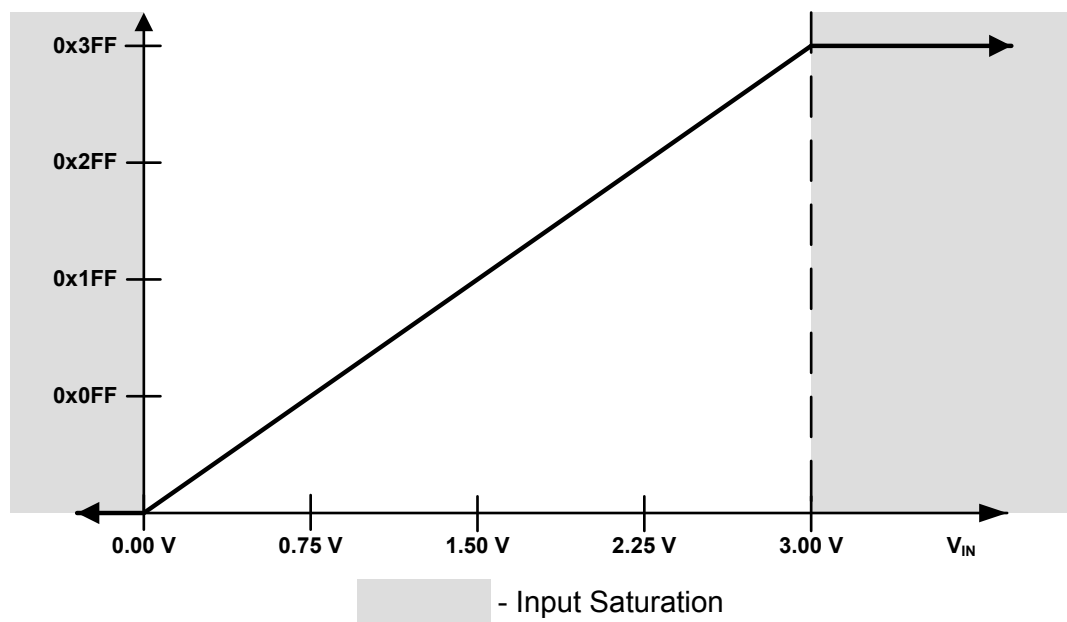


The ADC operates from both the 3.3-V analog and 1.2-V digital power supplies. The ADC clock can be configured to reduce power consumption when ADC conversions are not required (see “System Control” on page 212). The analog inputs are connected to the ADC through specially balanced input paths to minimize the distortion and cross-talk on the inputs. Detailed information on the ADC power supplies and analog inputs can be found in “Analog-to-Digital Converter (ADC)” on page 1325.

12.3.4.1 Internal Voltage Reference

The band-gap circuitry generates an internal 3.0 V reference that can be used by the ADC to produce a conversion value from the selected analog input. The range of this conversion value is from 0x000 to 0x3FF. This configuration results in a resolution of approximately 2.9 mV per ADC code. While the analog input pads can handle voltages beyond this range, the ADC conversions saturate in under-voltage and over-voltage cases. Figure 12-8 on page 613 shows the ADC conversion function of the analog inputs.

Figure 12-8. Internal Voltage Conversion Result



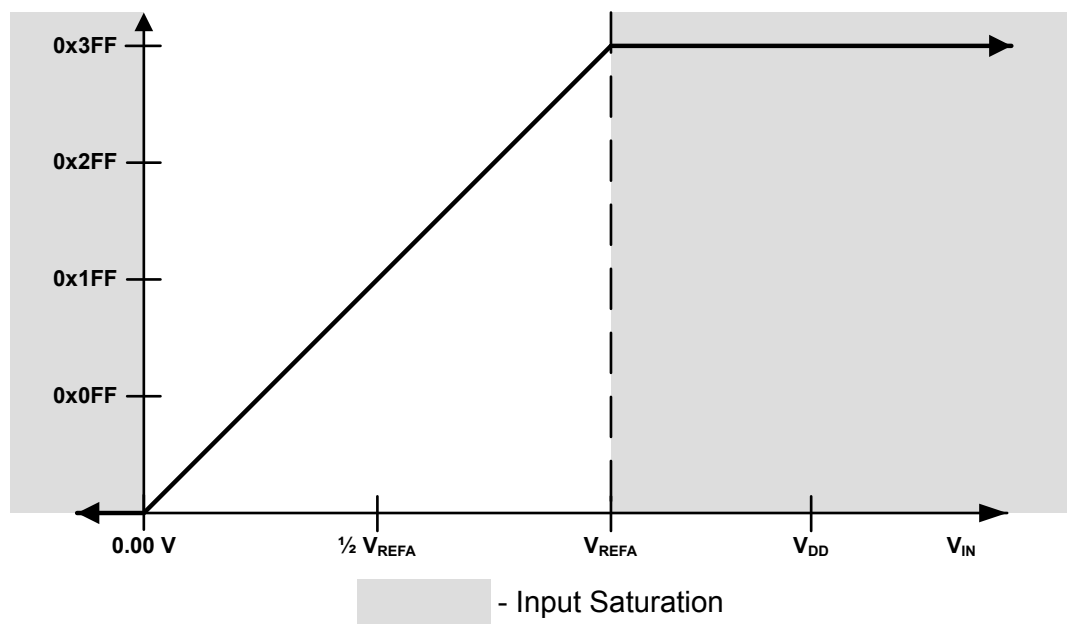
12.3.4.2 External Voltage Reference

The ADC can use an external voltage reference to produce the conversion value from the selected analog input by setting the V_{REF} bit in the **ADC Control (ADCCTL)** register. The V_{REF} bit specifies whether to use the internal or external reference. While the range of the conversion value remains the same (0x000 to 0x3FF), the analog voltage associated with the 0x3FF value corresponds to the value of the voltage when using the 3.0-V setting and three times the voltage when using the 1.0-V setting, resulting in a smaller voltage resolution per ADC code. Ground is always used as the reference level for the minimum conversion value. Analog input voltages above the external voltage reference saturate to 0x3FF while those below 0.0 V continue to saturate at 0x000. The V_{REFA} specification defines the useful range for the external voltage reference, see Table 26-23 on page 1326. Care must be taken to supply a reference voltage of acceptable quality.

Figure 12-9 on page 614 shows the ADC conversion function of the analog inputs when using an external voltage reference.

The external voltage reference can be more accurate than the internal reference by using a high-precision source or trimming the source.

Figure 12-9. External Voltage Conversion Result



12.3.5 Differential Sampling

In addition to traditional single-ended sampling, the ADC module supports differential sampling of two analog input channels. To enable differential sampling, software must set the D_n bit in the **ADCSSCTL0n** register in a step's configuration nibble.

When a sequence step is configured for differential sampling, the input pair to sample must be configured in the **ADCSSMUXn** register. Differential pair 0 samples analog inputs 0 and 1; differential pair 1 samples analog inputs 2 and 3; and so on (see Table 12-4 on page 614). The ADC does not support other differential pairings such as analog input 0 with analog input 3.

Table 12-4. Differential Sampling Pairs

Differential Pair	Analog Inputs
0	0 and 1
1	2 and 3
2	4 and 5
3	6 and 7
4	8 and 9
5	10 and 11
6	12 and 13
7	14 and 15

The voltage sampled in differential mode is the difference between the odd and even channels:

$$\Delta V \text{ (differential voltage)} = V_{IN_EVEN} \text{ (even channel)} - V_{IN_ODD} \text{ (odd channel)}, \text{ therefore:}$$

- If $\Delta V = 0$, then the conversion result = 0x1FF

- If $\Delta V > 0$, then the conversion result $> 0x1FF$ (range is $0x1FF-0x3FF$)
- If $\Delta V < 0$, then the conversion result $< 0x1FF$ (range is $0-0x1FF$)

The differential pairs assign polarities to the analog inputs: the even-numbered input is always positive, and the odd-numbered input is always negative. In order for a valid conversion result to appear, the negative input must be in the range of ± 1.5 V of the positive input. If an analog input is greater than 3 V or less than 0 V (the valid range for analog inputs), the input voltage is clipped, meaning it appears as either 3 V or 0 V, respectively, to the ADC.

Figure 12-10 on page 615 shows an example of the negative input centered at 1.5 V. In this configuration, the differential range spans from -1.5 V to 1.5 V. Figure 12-11 on page 616 shows an example where the negative input is centered at 0.75 V, meaning inputs on the positive input saturate past a differential voltage of -0.75 V because the input voltage is less than 0 V. Figure 12-12 on page 616 shows an example of the negative input centered at 2.25 V, where inputs on the positive channel saturate past a differential voltage of 0.75 V since the input voltage would be greater than 3 V.

Figure 12-10. Differential Sampling Range, $V_{IN_ODD} = 1.5$ V

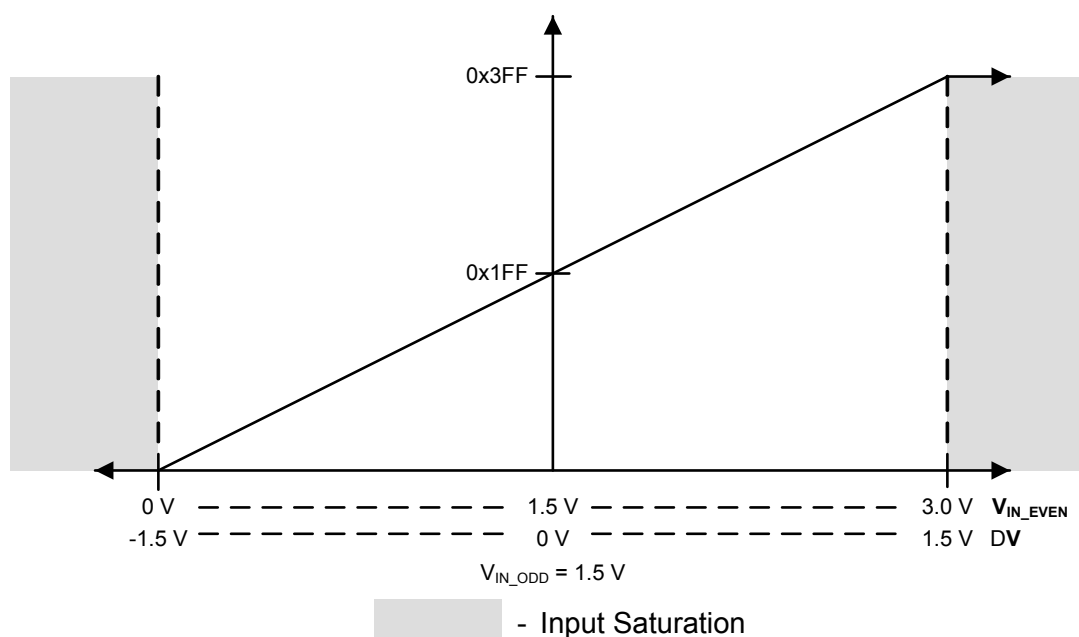
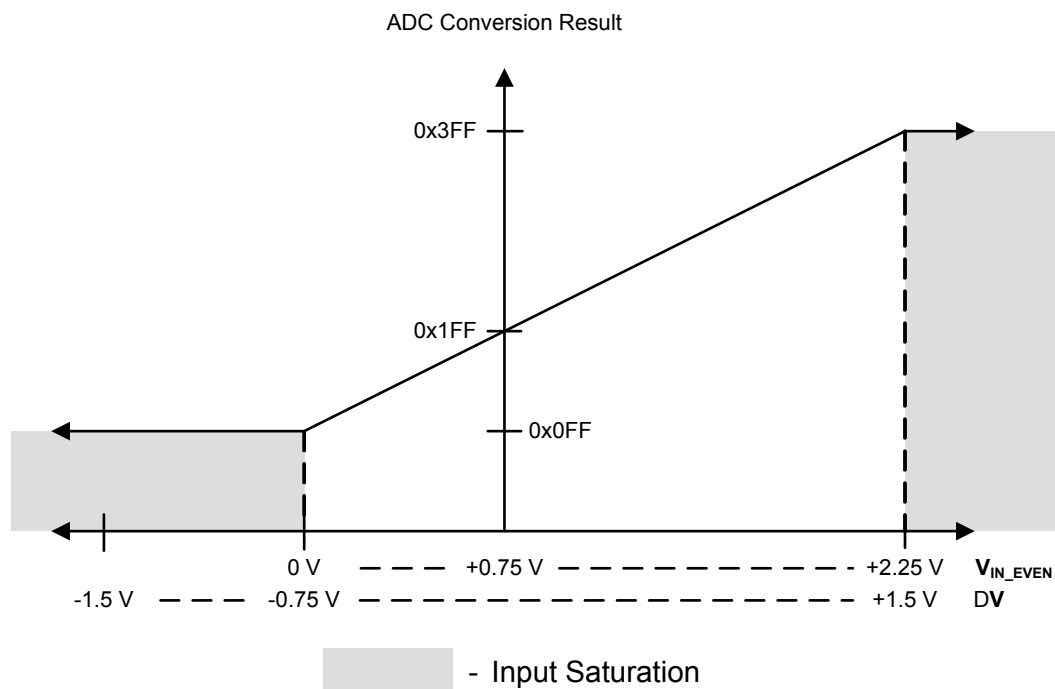
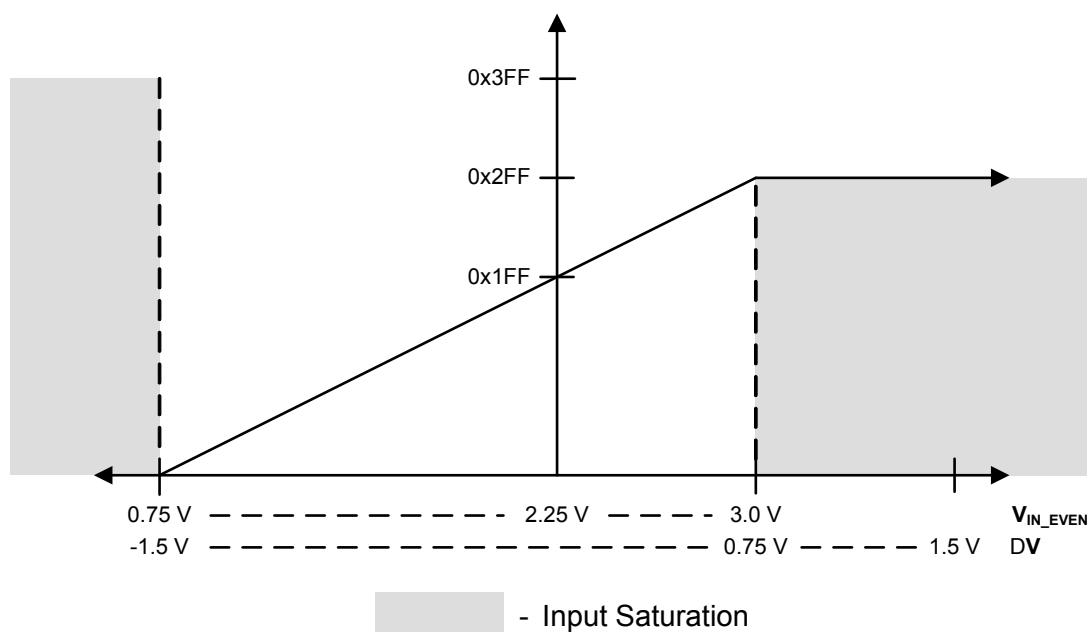


Figure 12-11. Differential Sampling Range, $V_{IN_ODD} = 0.75\text{ V}$ Figure 12-12. Differential Sampling Range, $V_{IN_ODD} = 2.25\text{ V}$ 

12.3.6 Internal Temperature Sensor

The temperature sensor's primary purpose is to notify the system that the internal temperature is too high or low for reliable operation.

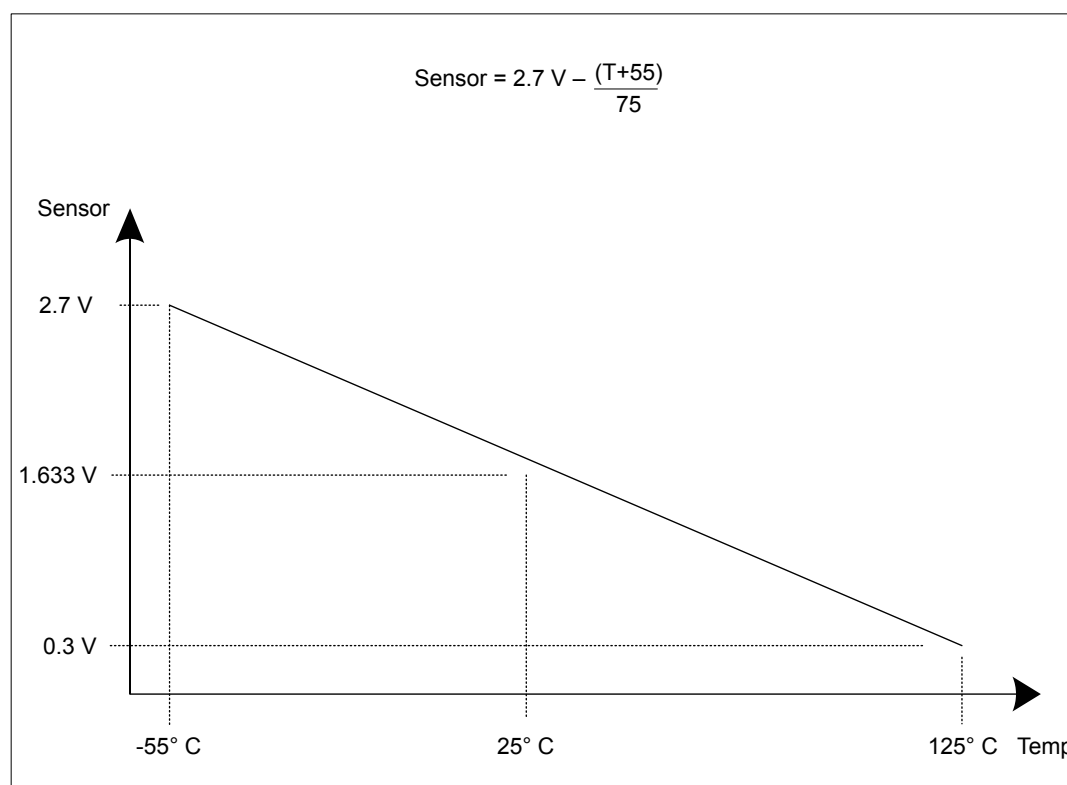
The temperature sensor does not have a separate enable, because it also contains the bandgap reference and must always be enabled. The reference is supplied to other analog modules; not just the ADC.

The internal temperature sensor provides an analog temperature reading as well as a reference voltage. This reference voltage, *SENSO*, is given by the following equation:

$$SENSO = 2.7 - ((T + 55) / 75)$$

This relation is shown in Figure 12-13 on page 617.

Figure 12-13. Internal Temperature Sensor Characteristic



The temperature sensor reading can be sampled in a sample sequence by setting the *TSn* bit in the **ADCSSCTLn** register. The temperature reading from the temperature sensor can also be given as a function of the ADC value. The following formula calculates temperature (in °C) based on the ADC reading:

$$\text{Temperature} = 147.5 - ((225 \times \text{ADC}) / 1023)$$

12.3.7 Digital Comparator Unit

An ADC is commonly used to sample an external signal and to monitor its value to ensure that it remains in a given range. To automate this monitoring procedure and reduce the amount of processor overhead that is required, each module provides eight digital comparators. Conversions from the ADC that are sent to the digital comparators are compared against the user programmable limits

in the **ADC Digital Comparator Range (ADCDCCMPn)** registers. If the observed signal moves out of the acceptable range, a processor interrupt can be generated and/or a trigger can be sent to the PWM module. The digital comparators four operational modes (Once, Always, Hysteresis Once, Hysteresis Always) can be applied to three separate regions (low band, mid band, high band) as defined by the user.

12.3.7.1 Output Functions

ADC conversions can either be stored in the ADC Sample Sequence FIFOs or compared using the digital comparator resources as defined by the S_nDCOP bits in the **ADC Sample Sequence n Operation (ADCSSOPn)** register. These selected ADC conversions are used by their respective digital comparator to monitor the external signal. Each comparator has two possible output functions: processor interrupts and triggers.

Each function has its own state machine to track the monitored signal. Even though the interrupt and trigger functions can be enabled individually or both at the same time, the same conversion data is used by each function to determine if the right conditions have been met to assert the associated output.

Interrupts

The digital comparator interrupt function is enabled by setting the CIE bit in the **ADC Digital Comparator Control (ADCDCCTLn)** register. This bit enables the interrupt function state machine to start monitoring the incoming ADC conversions. When the appropriate set of conditions is met, and the $DCONSS_x$ bit is set in the **ADCIM** register, an interrupt is sent to the interrupt controller.

Triggers

The digital comparator trigger function is enabled by setting the CTE bit in the **ADCDCCTLn** register. This bit enables the trigger function state machine to start monitoring the incoming ADC conversions. When the appropriate set of conditions is met, the corresponding digital comparator trigger to the PWM module is asserted.

12.3.7.2 Operational Modes

Four operational modes are provided to support a broad range of applications and multiple possible signaling requirements: Always, Once, Hysteresis Always, and Hysteresis Once. The operational mode is selected using the CIM or CTM field in the **ADCDCCTLn** register.

Always Mode

In the Always operational mode, the associated interrupt or trigger is asserted whenever the ADC conversion value meets its comparison criteria. The result is a string of assertions on the interrupt or trigger while the conversions are within the appropriate range.

Once Mode

In the Once operational mode, the associated interrupt or trigger is asserted whenever the ADC conversion value meets its comparison criteria, and the previous ADC conversion value did not. The result is a single assertion of the interrupt or trigger when the conversions are within the appropriate range.

Hysteresis-Always Mode

The Hysteresis-Always operational mode can only be used in conjunction with the low-band or high-band regions because the mid-band region must be crossed and the opposite region entered to clear the hysteresis condition. In the Hysteresis-Always mode, the associated interrupt or trigger

is asserted in the following cases: 1) the ADC conversion value meets its comparison criteria or 2) a previous ADC conversion value has met the comparison criteria, and the hysteresis condition has not been cleared by entering the opposite region. The result is a string of assertions on the interrupt or trigger that continue until the opposite region is entered.

Hysteresis-Once Mode

The Hysteresis-Once operational mode can only be used in conjunction with the low-band or high-band regions because the mid-band region must be crossed and the opposite region entered to clear the hysteresis condition. In the Hysteresis-Once mode, the associated interrupt or trigger is asserted only when the ADC conversion value meets its comparison criteria, the hysteresis condition is clear, and the previous ADC conversion did not meet the comparison criteria. The result is a single assertion on the interrupt or trigger.

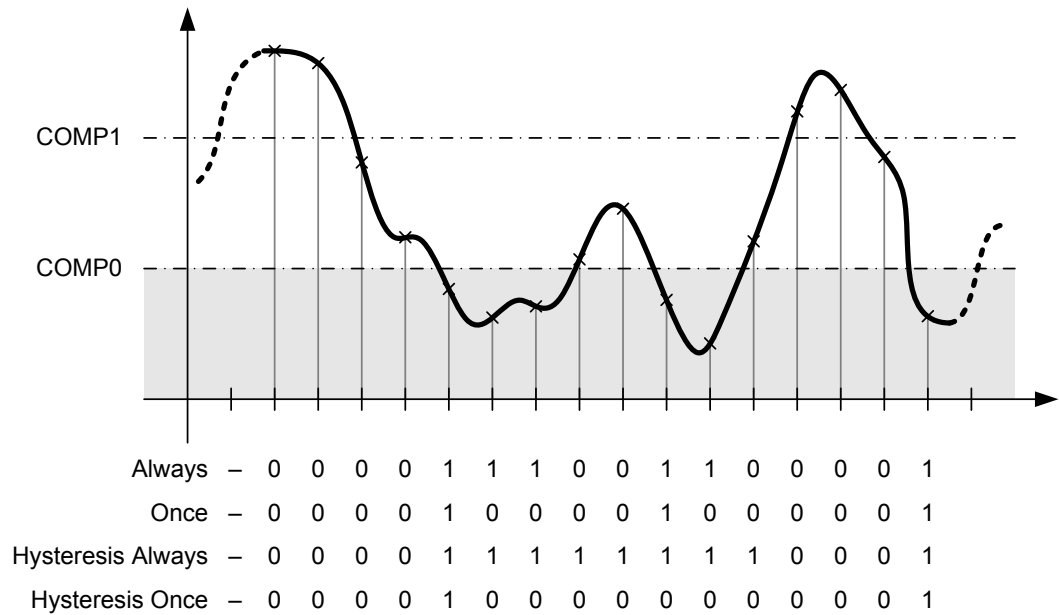
12.3.7.3 Function Ranges

The two comparison values, `COMP0` and `COMP1`, in the **ADC Digital Comparator Range (ADCDCCMPn)** register effectively break the conversion area into three distinct regions. These regions are referred to as the low-band (less than or equal to `COMP0`), mid-band (greater than `COMP0` but less than or equal to `COMP1`), and high-band (greater than `COMP1`) regions. `COMP0` and `COMP1` may be programmed to the same value, effectively creating two regions, but `COMP1` must always be greater than or equal to the value of `COMP0`. A `COMP1` value that is less than `COMP0` generates unpredictable results.

Low-Band Operation

To operate in the low-band region, either the `CIC` field or the `CTC` field in the **ADDCCTLn** register must be programmed to 0x0. This setting causes interrupts or triggers to be generated in the low-band region as defined by the programmed operational mode. An example of the state of the interrupt/trigger signal in the low-band region for each of the operational modes is shown in Figure 12-14 on page 620. Note that a "0" in a column following the operational mode name (Always, Once, Hysteresis Always, and Hysteresis Once) indicates that the interrupt or trigger signal is de-asserted and a "1" indicates that the signal is asserted.

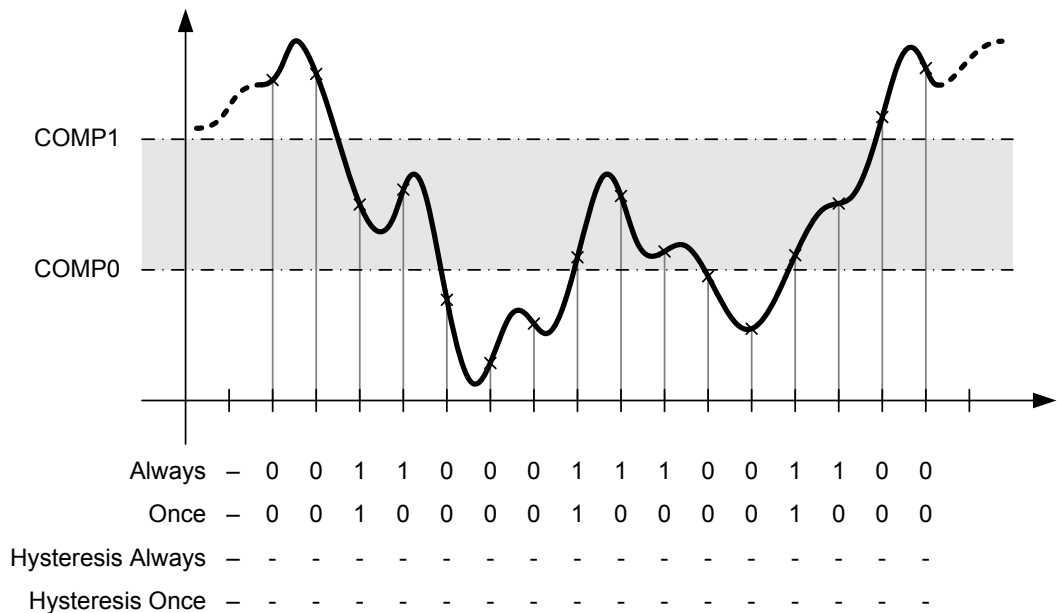
Figure 12-14. Low-Band Operation (CIC=0x0 and/or CTC=0x0)



Mid-Band Operation

To operate in the mid-band region, either the `CIC` field or the `CTC` field in the `ADDCCTLn` register must be programmed to 0x1. This setting causes interrupts or triggers to be generated in the mid-band region according the operation mode. Only the Always and Once operational modes are available in the mid-band region. An example of the state of the interrupt/trigger signal in the mid-band region for each of the allowed operational modes is shown in Figure 12-15 on page 621. Note that a "0" in a column following the operational mode name (Always or Once) indicates that the interrupt or trigger signal is de-asserted and a "1" indicates that the signal is asserted.

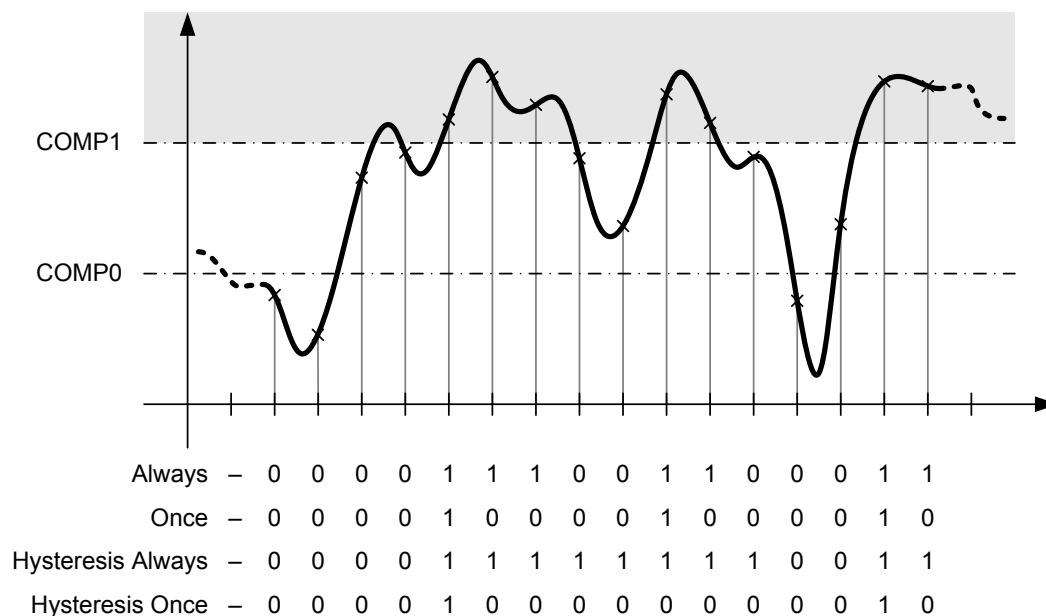
Figure 12-15. Mid-Band Operation (CIC=0x1 and/or CTC=0x1)



High-Band Operation

To operate in the high-band region, either the `CIC` field or the `CTC` field in the `ADCDCCTLn` register must be programmed to 0x3. This setting causes interrupts or triggers to be generated in the high-band region according the operation mode. An example of the state of the interrupt/trigger signal in the high-band region for each of the allowed operational modes is shown in Figure 12-16 on page 622. Note that a "0" in a column following the operational mode name (Always, Once, Hysteresis Always, and Hysteresis Once) indicates that the interrupt or trigger signal is de-asserted and a "1" indicates that the signal is asserted.

Figure 12-16. High-Band Operation (CIC=0x3 and/or CTC=0x3)



12.4 Initialization and Configuration

In order for the ADC module to be used, the PLL must be enabled and programmed to a supported crystal frequency in the **RCC** register (see page 228). Using unsupported frequencies can cause faulty operation in the ADC module.

12.4.1 Module Initialization

Initialization of the ADC module is a simple process with very few steps: enabling the clock to the ADC, disabling the analog isolation circuit associated with all inputs that are to be used, and reconfiguring the sample sequencer priorities (if needed).

The initialization sequence for the ADC is as follows:

1. Enable the ADC clock by using the **RCGC0** register (see page 271).
2. Enable the clock to the appropriate GPIO modules via the **RCGC2** register (see page 291). To find out which GPIO ports to enable, refer to “Signal Description” on page 605.
3. Set the GPIO **AFSEL** bits for the ADC input pins (see page 426). To determine which GPIOs to configure, see Table 24-4 on page 1254.
4. Configure the **AINx** and **VREFx** signals to be analog inputs by clearing the corresponding **DEN** bit in the **GPIO Digital Enable (GPIODEN)** register (see page 437).
5. Disable the analog isolation circuit for all ADC input pins that are to be used by writing a 1 to the appropriate bits of the **GPIOAMSEL** register (see page 442) in the associated GPIO block.

6. If required by the application, reconfigure the sample sequencer priorities in the **ADCSSPRI** register. The default configuration has Sample Sequencer 0 with the highest priority and Sample Sequencer 3 as the lowest priority.

12.4.2 Sample Sequencer Configuration

Configuration of the sample sequencers is slightly more complex than the module initialization because each sample sequencer is completely programmable.

The configuration for each sample sequencer should be as follows:

1. Ensure that the sample sequencer is disabled by clearing the corresponding **ASENn** bit in the **ADCACTSS** register. Programming of the sample sequencers is allowed without having them enabled. Disabling the sequencer during programming prevents erroneous execution if a trigger event were to occur during the configuration process.
2. Configure the trigger event for the sample sequencer in the **ADCEMUX** register.
3. For each sample in the sample sequence, configure the corresponding input source in the **ADCSSMUXn** register.
4. For each sample in the sample sequence, configure the sample control bits in the corresponding nibble in the **ADCSSCTLn** register. When programming the last nibble, ensure that the **END** bit is set. Failure to set the **END** bit causes unpredictable behavior.
5. If interrupts are to be used, set the corresponding **MASK** bit in the **ADCIM** register.
6. Enable the sample sequencer logic by setting the corresponding **ASENn** bit in the **ADCACTSS** register.

12.5 Register Map

Table 12-5 on page 623 lists the ADC registers. The offset listed is a hexadecimal increment to the register's address, relative to that ADC module's base address of:

- ADC0: 0x4003.8000
- ADC1: 0x4003.9000

Note that the ADC module clock must be enabled before the registers can be programmed (see page 271). There must be a delay of 3 system clocks after the ADC module clock is enabled before any ADC module registers are accessed.

Table 12-5. ADC Register Map

Offset	Name	Type	Reset	Description	See page
0x000	ADCACTSS	R/W	0x0000.0000	ADC Active Sample Sequencer	626
0x004	ADCRIS	RO	0x0000.0000	ADC Raw Interrupt Status	627
0x008	ADCIM	R/W	0x0000.0000	ADC Interrupt Mask	629
0x00C	ADCISC	R/W1C	0x0000.0000	ADC Interrupt Status and Clear	631
0x010	ADCOSTAT	R/W1C	0x0000.0000	ADC Overflow Status	634
0x014	ADCEMUX	R/W	0x0000.0000	ADC Event Multiplexer Select	636

Table 12-5. ADC Register Map (continued)

Offset	Name	Type	Reset	Description	See page
0x018	ADCUSTAT	R/W1C	0x0000.0000	ADC Underflow Status	641
0x020	ADCSSPRI	R/W	0x0000.3210	ADC Sample Sequencer Priority	642
0x024	ADCSPC	R/W	0x0000.0000	ADC Sample Phase Control	644
0x028	ADCPSSI	R/W	-	ADC Processor Sample Sequence Initiate	646
0x030	ADCSAC	R/W	0x0000.0000	ADC Sample Averaging Control	648
0x034	ADCDCISC	R/W1C	0x0000.0000	ADC Digital Comparator Interrupt Status and Clear	649
0x038	ADCCTL	R/W	0x0000.0000	ADC Control	651
0x040	ADCSSMUX0	R/W	0x0000.0000	ADC Sample Sequence Input Multiplexer Select 0	652
0x044	ADCSSCTL0	R/W	0x0000.0000	ADC Sample Sequence Control 0	654
0x048	ADCSSFIFO0	RO	-	ADC Sample Sequence Result FIFO 0	657
0x04C	ADCSSFSTAT0	RO	0x0000.0100	ADC Sample Sequence FIFO 0 Status	658
0x050	ADCSSOP0	R/W	0x0000.0000	ADC Sample Sequence 0 Operation	660
0x054	ADCSSDC0	R/W	0x0000.0000	ADC Sample Sequence 0 Digital Comparator Select	662
0x060	ADCSSMUX1	R/W	0x0000.0000	ADC Sample Sequence Input Multiplexer Select 1	664
0x064	ADCSSCTL1	R/W	0x0000.0000	ADC Sample Sequence Control 1	665
0x068	ADCSSFIFO1	RO	-	ADC Sample Sequence Result FIFO 1	657
0x06C	ADCSSFSTAT1	RO	0x0000.0100	ADC Sample Sequence FIFO 1 Status	658
0x070	ADCSSOP1	R/W	0x0000.0000	ADC Sample Sequence 1 Operation	667
0x074	ADCSSDC1	R/W	0x0000.0000	ADC Sample Sequence 1 Digital Comparator Select	668
0x080	ADCSSMUX2	R/W	0x0000.0000	ADC Sample Sequence Input Multiplexer Select 2	664
0x084	ADCSSCTL2	R/W	0x0000.0000	ADC Sample Sequence Control 2	665
0x088	ADCSSFIFO2	RO	-	ADC Sample Sequence Result FIFO 2	657
0x08C	ADCSSFSTAT2	RO	0x0000.0100	ADC Sample Sequence FIFO 2 Status	658
0x090	ADCSSOP2	R/W	0x0000.0000	ADC Sample Sequence 2 Operation	667
0x094	ADCSSDC2	R/W	0x0000.0000	ADC Sample Sequence 2 Digital Comparator Select	668
0x0A0	ADCSSMUX3	R/W	0x0000.0000	ADC Sample Sequence Input Multiplexer Select 3	670
0x0A4	ADCSSCTL3	R/W	0x0000.0002	ADC Sample Sequence Control 3	671
0x0A8	ADCSSFIFO3	RO	-	ADC Sample Sequence Result FIFO 3	657
0x0AC	ADCSSFSTAT3	RO	0x0000.0100	ADC Sample Sequence FIFO 3 Status	658
0x0B0	ADCSSOP3	R/W	0x0000.0000	ADC Sample Sequence 3 Operation	672
0x0B4	ADCSSDC3	R/W	0x0000.0000	ADC Sample Sequence 3 Digital Comparator Select	673
0xD00	ADCDCRIC	R/W	0x0000.0000	ADC Digital Comparator Reset Initial Conditions	674

Table 12-5. ADC Register Map (continued)

Offset	Name	Type	Reset	Description	See page
0xE00	ADCDCTL0	R/W	0x0000.0000	ADC Digital Comparator Control 0	679
0xE04	ADCDCTL1	R/W	0x0000.0000	ADC Digital Comparator Control 1	679
0xE08	ADCDCTL2	R/W	0x0000.0000	ADC Digital Comparator Control 2	679
0xE0C	ADCDCTL3	R/W	0x0000.0000	ADC Digital Comparator Control 3	679
0xE10	ADCDCTL4	R/W	0x0000.0000	ADC Digital Comparator Control 4	679
0xE14	ADCDCTL5	R/W	0x0000.0000	ADC Digital Comparator Control 5	679
0xE18	ADCDCTL6	R/W	0x0000.0000	ADC Digital Comparator Control 6	679
0xE1C	ADCDCTL7	R/W	0x0000.0000	ADC Digital Comparator Control 7	679
0xE40	ADCDCOMP0	R/W	0x0000.0000	ADC Digital Comparator Range 0	682
0xE44	ADCDCOMP1	R/W	0x0000.0000	ADC Digital Comparator Range 1	682
0xE48	ADCDCOMP2	R/W	0x0000.0000	ADC Digital Comparator Range 2	682
0xE4C	ADCDCOMP3	R/W	0x0000.0000	ADC Digital Comparator Range 3	682
0xE50	ADCDCOMP4	R/W	0x0000.0000	ADC Digital Comparator Range 4	682
0xE54	ADCDCOMP5	R/W	0x0000.0000	ADC Digital Comparator Range 5	682
0xE58	ADCDCOMP6	R/W	0x0000.0000	ADC Digital Comparator Range 6	682
0xE5C	ADCDCOMP7	R/W	0x0000.0000	ADC Digital Comparator Range 7	682

12.6 Register Descriptions

The remainder of this section lists and describes the ADC registers, in numerical order by address offset.

Register 1: ADC Active Sample Sequencer (ADCACTSS), offset 0x000

This register controls the activation of the sample sequencers. Each sample sequencer can be enabled or disabled independently.

ADC Active Sample Sequencer (ADCACTSS)

ADC0 base: 0x4003.8000

ADC1 base: 0x4003.9000

Offset 0x000

Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved												ASEN3	ASEN2	ASEN1	ASEN0
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:4	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
3	ASEN3	R/W	0	ADC SS3 Enable Value Description 1 Sample Sequencer 3 is enabled. 0 Sample Sequencer 3 is disabled.
2	ASEN2	R/W	0	ADC SS2 Enable Value Description 1 Sample Sequencer 2 is enabled. 0 Sample Sequencer 2 is disabled.
1	ASEN1	R/W	0	ADC SS1 Enable Value Description 1 Sample Sequencer 1 is enabled. 0 Sample Sequencer 1 is disabled.
0	ASEN0	R/W	0	ADC SS0 Enable Value Description 1 Sample Sequencer 0 is enabled. 0 Sample Sequencer 0 is disabled.

Register 2: ADC Raw Interrupt Status (ADCRIS), offset 0x004

This register shows the status of the raw interrupt signal of each sample sequencer. These bits may be polled by software to look for interrupt conditions without sending the interrupts to the interrupt controller.

ADC Raw Interrupt Status (ADCRIS)

ADC0 base: 0x4003.8000
 ADC1 base: 0x4003.9000
 Offset 0x004
 Type RO, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															INRDC
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved												INR3	INR2	INR1	INR0
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:17	reserved	RO	0x000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
16	INRDC	RO	0	Digital Comparator Raw Interrupt Status Value Description 1 At least one bit in the ADCDISC register is set, meaning that a digital comparator interrupt has occurred. 0 All bits in the ADCDISC register are clear.
15:4	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
3	INR3	RO	0	SS3 Raw Interrupt Status Value Description 1 A sample has completed conversion and the respective ADCSSCTL3 IE_n bit is set, enabling a raw interrupt. 0 An interrupt has not occurred. This bit is cleared by writing a 1 to the IN3 bit in the ADCISC register.
2	INR2	RO	0	SS2 Raw Interrupt Status Value Description 1 A sample has completed conversion and the respective ADCSSCTL2 IE_n bit is set, enabling a raw interrupt. 0 An interrupt has not occurred. This bit is cleared by writing a 1 to the IN2 bit in the ADCISC register.

Bit/Field	Name	Type	Reset	Description
1	INR1	RO	0	SS1 Raw Interrupt Status Value Description 1 A sample has completed conversion and the respective ADCSSCTL1 IE_n bit is set, enabling a raw interrupt. 0 An interrupt has not occurred. This bit is cleared by writing a 1 to the $IN1$ bit in the ADCISC register.
0	INR0	RO	0	SS0 Raw Interrupt Status Value Description 1 A sample has completed conversion and the respective ADCSSCTL0 IE_n bit is set, enabling a raw interrupt. 0 An interrupt has not occurred. This bit is cleared by writing a 1 to the $IN0$ bit in the ADCISC register.

Register 3: ADC Interrupt Mask (ADCIM), offset 0x008

This register controls whether the sample sequencer and digital comparator raw interrupt signals are sent to the interrupt controller. Each raw interrupt signal can be masked independently. Only a single DCONSS_n bit should be set at any given time. Setting more than one of these bits results in the INRDC bit from the ACDRIS register being masked, and no interrupt is generated on any of the sample sequencer interrupt lines.

ADC Interrupt Mask (ADCIM)

ADC0 base: 0x4003.8000

ADC1 base: 0x4003.9000

Offset 0x008

Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved												DCONSS3	DCONSS2	DCONSS1	DCONSS0
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved												MASK3	MASK2	MASK1	MASK0
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:20	reserved	RO	0x000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
19	DCONSS3	R/W	0	Digital Comparator Interrupt on SS3 Value Description 1 The raw interrupt signal from the digital comparators (INRDC bit in the ADCRIS register) is sent to the interrupt controller on the SS3 interrupt line. 0 The status of the digital comparators does not affect the SS3 interrupt status.
18	DCONSS2	R/W	0	Digital Comparator Interrupt on SS2 Value Description 1 The raw interrupt signal from the digital comparators (INRDC bit in the ADCRIS register) is sent to the interrupt controller on the SS2 interrupt line. 0 The status of the digital comparators does not affect the SS2 interrupt status.
17	DCONSS1	R/W	0	Digital Comparator Interrupt on SS1 Value Description 1 The raw interrupt signal from the digital comparators (INRDC bit in the ADCRIS register) is sent to the interrupt controller on the SS1 interrupt line. 0 The status of the digital comparators does not affect the SS1 interrupt status.

Bit/Field	Name	Type	Reset	Description
16	DCONSS0	R/W	0	Digital Comparator Interrupt on SS0 Value Description 1 The raw interrupt signal from the digital comparators (<i>INRDC</i> bit in the ADCRIS register) is sent to the interrupt controller on the SS0 interrupt line. 0 The status of the digital comparators does not affect the SS0 interrupt status.
15:4	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
3	MASK3	R/W	0	SS3 Interrupt Mask Value Description 1 The raw interrupt signal from Sample Sequencer 3 (ADCRIS register <i>INR3</i> bit) is sent to the interrupt controller. 0 The status of Sample Sequencer 3 does not affect the SS3 interrupt status.
2	MASK2	R/W	0	SS2 Interrupt Mask Value Description 1 The raw interrupt signal from Sample Sequencer 2 (ADCRIS register <i>INR2</i> bit) is sent to the interrupt controller. 0 The status of Sample Sequencer 2 does not affect the SS2 interrupt status.
1	MASK1	R/W	0	SS1 Interrupt Mask Value Description 1 The raw interrupt signal from Sample Sequencer 1 (ADCRIS register <i>INR1</i> bit) is sent to the interrupt controller. 0 The status of Sample Sequencer 1 does not affect the SS1 interrupt status.
0	MASK0	R/W	0	SS0 Interrupt Mask Value Description 1 The raw interrupt signal from Sample Sequencer 0 (ADCRIS register <i>INR0</i> bit) is sent to the interrupt controller. 0 The status of Sample Sequencer 0 does not affect the SS0 interrupt status.

Register 4: ADC Interrupt Status and Clear (ADCISC), offset 0x00C

This register provides the mechanism for clearing sample sequencer interrupt conditions and shows the status of interrupts generated by the sample sequencers and the digital comparators which have been sent to the interrupt controller. When read, each bit field is the logical AND of the respective **INR** and **MASK** bits. Sample sequencer interrupts are cleared by writing a 1 to the corresponding bit position. Digital comparator interrupts are cleared by writing a 1 to the appropriate bits in the **ADCDCISC** register. If software is polling the **ADCRIS** instead of generating interrupts, the sample sequence **INR_n** bits are still cleared via the **ADCISC** register, even if the **IN_n** bit is not set.

ADC Interrupt Status and Clear (ADCISC)

ADC0 base: 0x4003.8000

ADC1 base: 0x4003.9000

Offset 0x00C

Type R/W1C, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved												DCINSS3	DCINSS2	DCINSS1	DCINSS0
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved												IN3	IN2	IN1	IN0
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W1C	R/W1C	R/W1C	R/W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:20	reserved	RO	0x000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
19	DCINSS3	RO	0	Digital Comparator Interrupt Status on SS3 Value Description 1 Both the INRDC bit in the ADCRIS register and the DCONSS3 bit in the ADCIM register are set, providing a level-based interrupt to the interrupt controller. 0 No interrupt has occurred or the interrupt is masked. This bit is cleared by writing a 1 to it. Clearing this bit also clears the INRDC bit in the ADCRIS register.
18	DCINSS2	RO	0	Digital Comparator Interrupt Status on SS2 Value Description 1 Both the INRDC bit in the ADCRIS register and the DCONSS2 bit in the ADCIM register are set, providing a level-based interrupt to the interrupt controller. 0 No interrupt has occurred or the interrupt is masked. This bit is cleared by writing a 1 to it. Clearing this bit also clears the INRDC bit in the ADCRIS register.

Bit/Field	Name	Type	Reset	Description
17	DCINSS1	RO	0	Digital Comparator Interrupt Status on SS1 Value Description 1 Both the <code>INRDC</code> bit in the ADCRIS register and the <code>DCONSS1</code> bit in the ADCIM register are set, providing a level-based interrupt to the interrupt controller. 0 No interrupt has occurred or the interrupt is masked. This bit is cleared by writing a 1 to it. Clearing this bit also clears the <code>INRDC</code> bit in the ADCRIS register.
16	DCINSS0	RO	0	Digital Comparator Interrupt Status on SS0 Value Description 1 Both the <code>INRDC</code> bit in the ADCRIS register and the <code>DCONSS0</code> bit in the ADCIM register are set, providing a level-based interrupt to the interrupt controller. 0 No interrupt has occurred or the interrupt is masked. This bit is cleared by writing a 1 to it. Clearing this bit also clears the <code>INRDC</code> bit in the ADCRIS register.
15:4	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
3	IN3	R/W1C	0	SS3 Interrupt Status and Clear Value Description 1 Both the <code>INR3</code> bit in the ADCRIS register and the <code>MASK3</code> bit in the ADCIM register are set, providing a level-based interrupt to the interrupt controller. 0 No interrupt has occurred or the interrupt is masked. This bit is cleared by writing a 1. Clearing this bit also clears the <code>INR3</code> bit in the ADCRIS register.
2	IN2	R/W1C	0	SS2 Interrupt Status and Clear Value Description 1 Both the <code>INR2</code> bit in the ADCRIS register and the <code>MASK2</code> bit in the ADCIM register are set, providing a level-based interrupt to the interrupt controller. 0 No interrupt has occurred or the interrupt is masked. This bit is cleared by writing a 1. Clearing this bit also clears the <code>INR2</code> bit in the ADCRIS register.

Bit/Field	Name	Type	Reset	Description
1	IN1	R/W1C	0	SS1 Interrupt Status and Clear Value Description 1 Both the <code>INR1</code> bit in the ADCRIS register and the <code>MASK1</code> bit in the ADCIM register are set, providing a level-based interrupt to the interrupt controller. 0 No interrupt has occurred or the interrupt is masked. This bit is cleared by writing a 1. Clearing this bit also clears the <code>INR1</code> bit in the ADCRIS register.
0	IN0	R/W1C	0	SS0 Interrupt Status and Clear Value Description 1 Both the <code>INR0</code> bit in the ADCRIS register and the <code>MASK0</code> bit in the ADCIM register are set, providing a level-based interrupt to the interrupt controller. 0 No interrupt has occurred or the interrupt is masked. This bit is cleared by writing a 1. Clearing this bit also clears the <code>INR0</code> bit in the ADCRIS register.

Register 5: ADC Overflow Status (ADCOSTAT), offset 0x010

This register indicates overflow conditions in the sample sequencer FIFOs. Once the overflow condition has been handled by software, the condition can be cleared by writing a 1 to the corresponding bit position.

ADC Overflow Status (ADCOSTAT)

ADC0 base: 0x4003.8000

ADC1 base: 0x4003.9000

Offset 0x010

Type R/W1C, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved												OV3	OV2	OV1	OV0
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W1C	R/W1C	R/W1C	R/W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:4	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
3	OV3	R/W1C	0	SS3 FIFO Overflow Value Description 1 The FIFO for Sample Sequencer 3 has hit an overflow condition, meaning that the FIFO is full and a write was requested. When an overflow is detected, the most recent write is dropped. 0 The FIFO has not overflowed. This bit is cleared by writing a 1.
2	OV2	R/W1C	0	SS2 FIFO Overflow Value Description 1 The FIFO for Sample Sequencer 2 has hit an overflow condition, meaning that the FIFO is full and a write was requested. When an overflow is detected, the most recent write is dropped. 0 The FIFO has not overflowed. This bit is cleared by writing a 1.
1	OV1	R/W1C	0	SS1 FIFO Overflow Value Description 1 The FIFO for Sample Sequencer 1 has hit an overflow condition, meaning that the FIFO is full and a write was requested. When an overflow is detected, the most recent write is dropped. 0 The FIFO has not overflowed. This bit is cleared by writing a 1.

Bit/Field	Name	Type	Reset	Description
0	OV0	R/W1C	0	SS0 FIFO Overflow
				Value Description
				1 The FIFO for Sample Sequencer 0 has hit an overflow condition, meaning that the FIFO is full and a write was requested. When an overflow is detected, the most recent write is dropped.
				0 The FIFO has not overflowed.
				This bit is cleared by writing a 1.

Register 6: ADC Event Multiplexer Select (ADCEMUX), offset 0x014

The **ADCEMUX** selects the event (trigger) that initiates sampling for each sample sequencer. Each sample sequencer can be configured with a unique trigger source.

ADC Event Multiplexer Select (ADCEMUX)

ADC0 base: 0x4003.8000

ADC1 base: 0x4003.9000

Offset 0x014

Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EM3				EM2				EM1				EM0			
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:16	reserved	RO	0x0000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

Bit/Field	Name	Type	Reset	Description																																
15:12	EM3	R/W	0x0	SS3 Trigger Select This field selects the trigger source for Sample Sequencer 3. The valid configurations for this field are: <table><tr><th>Value</th><th>Event</th></tr><tr><td>0x0</td><td> Processor (default) The trigger is initiated by setting the <code>SS_n</code> bit in the ADCPSSI register. </td></tr><tr><td>0x1</td><td> Analog Comparator 0 This trigger is configured by the Analog Comparator Control 0 (ACCTL0) register (page 1127). </td></tr><tr><td>0x2</td><td> Analog Comparator 1 This trigger is configured by the Analog Comparator Control 1 (ACCTL1) register (page 1127). </td></tr><tr><td>0x3</td><td> Analog Comparator 2 This trigger is configured by the Analog Comparator Control 2 (ACCTL2) register (page 1127). </td></tr><tr><td>0x4</td><td> External (GPIO <code>PB4</code>) This trigger is connected to the GPIO interrupt for <code>PB4</code> (see “ADC Trigger Source” on page 410). Note: <code>PB4</code> can be used to trigger the ADC. However, the <code>PB4/AIN10</code> pin cannot be used as both a GPIO and an analog input. </td></tr><tr><td>0x5</td><td> Timer In addition, the trigger must be enabled with the <code>TnOTE</code> bit in the GPTMCTL register (page 553). </td></tr><tr><td>0x6</td><td> PWM0 The PWM generator 0 trigger can be configured with the PWM0 Interrupt and Trigger Enable (PWM0INTEN) register (page 1174). </td></tr><tr><td>0x7</td><td> PWM1 The PWM generator 1 trigger can be configured with the PWM1INTEN register (page 1174). </td></tr><tr><td>0x8</td><td> PWM2 The PWM generator 2 trigger can be configured with the PWM2INTEN register (page 1174). </td></tr><tr><td>0x9</td><td> PWM3 The PWM generator 3 trigger can be configured with the PWM3INTEN register (page 1174). </td></tr><tr><td>0xA-0xE</td><td>reserved</td><td></td><td></td><td></td></tr><tr><td>0xF</td><td>Always (continuously sample)</td><td></td><td></td><td></td></tr></table>	Value	Event	0x0	Processor (default) The trigger is initiated by setting the <code>SS_n</code> bit in the ADCPSSI register.	0x1	Analog Comparator 0 This trigger is configured by the Analog Comparator Control 0 (ACCTL0) register (page 1127).	0x2	Analog Comparator 1 This trigger is configured by the Analog Comparator Control 1 (ACCTL1) register (page 1127).	0x3	Analog Comparator 2 This trigger is configured by the Analog Comparator Control 2 (ACCTL2) register (page 1127).	0x4	External (GPIO <code>PB4</code>) This trigger is connected to the GPIO interrupt for <code>PB4</code> (see “ADC Trigger Source” on page 410). Note: <code>PB4</code> can be used to trigger the ADC. However, the <code>PB4/AIN10</code> pin cannot be used as both a GPIO and an analog input.	0x5	Timer In addition, the trigger must be enabled with the <code>TnOTE</code> bit in the GPTMCTL register (page 553).	0x6	PWM0 The PWM generator 0 trigger can be configured with the PWM0 Interrupt and Trigger Enable (PWM0INTEN) register (page 1174).	0x7	PWM1 The PWM generator 1 trigger can be configured with the PWM1INTEN register (page 1174).	0x8	PWM2 The PWM generator 2 trigger can be configured with the PWM2INTEN register (page 1174).	0x9	PWM3 The PWM generator 3 trigger can be configured with the PWM3INTEN register (page 1174).	0xA-0xE	reserved				0xF	Always (continuously sample)			
Value	Event																																			
0x0	Processor (default) The trigger is initiated by setting the <code>SS_n</code> bit in the ADCPSSI register.																																			
0x1	Analog Comparator 0 This trigger is configured by the Analog Comparator Control 0 (ACCTL0) register (page 1127).																																			
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0x7	PWM1 The PWM generator 1 trigger can be configured with the PWM1INTEN register (page 1174).																																			
0x8	PWM2 The PWM generator 2 trigger can be configured with the PWM2INTEN register (page 1174).																																			
0x9	PWM3 The PWM generator 3 trigger can be configured with the PWM3INTEN register (page 1174).																																			
0xA-0xE	reserved																																			
0xF	Always (continuously sample)																																			

Bit/Field	Name	Type	Reset	Description																																
11:8	EM2	R/W	0x0	SS2 Trigger Select This field selects the trigger source for Sample Sequencer 2. The valid configurations for this field are: <table><tr><th>Value</th><th>Event</th></tr><tr><td>0x0</td><td> Processor (default) The trigger is initiated by setting the <code>SSn</code> bit in the ADCPSSI register. </td></tr><tr><td>0x1</td><td> Analog Comparator 0 This trigger is configured by the Analog Comparator Control 0 (ACCTL0) register (page 1127). </td></tr><tr><td>0x2</td><td> Analog Comparator 1 This trigger is configured by the Analog Comparator Control 1 (ACCTL1) register (page 1127). </td></tr><tr><td>0x3</td><td> Analog Comparator 2 This trigger is configured by the Analog Comparator Control 2 (ACCTL2) register (page 1127). </td></tr><tr><td>0x4</td><td> External (GPIO <code>PB4</code>) This trigger is connected to the GPIO interrupt for <code>PB4</code> (see “ADC Trigger Source” on page 410). Note: <code>PB4</code> can be used to trigger the ADC. However, the <code>PB4/AIN10</code> pin cannot be used as both a GPIO and an analog input. </td></tr><tr><td>0x5</td><td> Timer In addition, the trigger must be enabled with the <code>TnOTE</code> bit in the GPTMCTL register (page 553). </td></tr><tr><td>0x6</td><td> PWM0 The PWM generator 0 trigger can be configured with the PWM0 Interrupt and Trigger Enable (PWM0INTEN) register (page 1174). </td></tr><tr><td>0x7</td><td> PWM1 The PWM generator 1 trigger can be configured with the PWM1INTEN register (page 1174). </td></tr><tr><td>0x8</td><td> PWM2 The PWM generator 2 trigger can be configured with the PWM2INTEN register (page 1174). </td></tr><tr><td>0x9</td><td> PWM3 The PWM generator 3 trigger can be configured with the PWM3INTEN register (page 1174). </td></tr><tr><td>0xA-0xE</td><td>reserved</td><td></td><td></td><td></td></tr><tr><td>0xF</td><td>Always (continuously sample)</td><td></td><td></td><td></td></tr></table>	Value	Event	0x0	Processor (default) The trigger is initiated by setting the <code>SSn</code> bit in the ADCPSSI register.	0x1	Analog Comparator 0 This trigger is configured by the Analog Comparator Control 0 (ACCTL0) register (page 1127).	0x2	Analog Comparator 1 This trigger is configured by the Analog Comparator Control 1 (ACCTL1) register (page 1127).	0x3	Analog Comparator 2 This trigger is configured by the Analog Comparator Control 2 (ACCTL2) register (page 1127).	0x4	External (GPIO <code>PB4</code>) This trigger is connected to the GPIO interrupt for <code>PB4</code> (see “ADC Trigger Source” on page 410). Note: <code>PB4</code> can be used to trigger the ADC. However, the <code>PB4/AIN10</code> pin cannot be used as both a GPIO and an analog input.	0x5	Timer In addition, the trigger must be enabled with the <code>TnOTE</code> bit in the GPTMCTL register (page 553).	0x6	PWM0 The PWM generator 0 trigger can be configured with the PWM0 Interrupt and Trigger Enable (PWM0INTEN) register (page 1174).	0x7	PWM1 The PWM generator 1 trigger can be configured with the PWM1INTEN register (page 1174).	0x8	PWM2 The PWM generator 2 trigger can be configured with the PWM2INTEN register (page 1174).	0x9	PWM3 The PWM generator 3 trigger can be configured with the PWM3INTEN register (page 1174).	0xA-0xE	reserved				0xF	Always (continuously sample)			
Value	Event																																			
0x0	Processor (default) The trigger is initiated by setting the <code>SSn</code> bit in the ADCPSSI register.																																			
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0x3	Analog Comparator 2 This trigger is configured by the Analog Comparator Control 2 (ACCTL2) register (page 1127).																																			
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0x9	PWM3 The PWM generator 3 trigger can be configured with the PWM3INTEN register (page 1174).																																			
0xA-0xE	reserved																																			
0xF	Always (continuously sample)																																			

Bit/Field	Name	Type	Reset	Description																																
7:4	EM1	R/W	0x0	SS1 Trigger Select This field selects the trigger source for Sample Sequencer 1. The valid configurations for this field are: <table><tr><th>Value</th><th>Event</th></tr><tr><td>0x0</td><td> Processor (default) The trigger is initiated by setting the <code>SSn</code> bit in the ADCPSSI register. </td></tr><tr><td>0x1</td><td> Analog Comparator 0 This trigger is configured by the Analog Comparator Control 0 (ACCTL0) register (page 1127). </td></tr><tr><td>0x2</td><td> Analog Comparator 1 This trigger is configured by the Analog Comparator Control 1 (ACCTL1) register (page 1127). </td></tr><tr><td>0x3</td><td> Analog Comparator 2 This trigger is configured by the Analog Comparator Control 2 (ACCTL2) register (page 1127). </td></tr><tr><td>0x4</td><td> External (GPIO <code>PB4</code>) This trigger is connected to the GPIO interrupt for <code>PB4</code> (see “ADC Trigger Source” on page 410). Note: <code>PB4</code> can be used to trigger the ADC. However, the <code>PB4/AIN10</code> pin cannot be used as both a GPIO and an analog input. </td></tr><tr><td>0x5</td><td> Timer In addition, the trigger must be enabled with the <code>TnOTE</code> bit in the GPTMCTL register (page 553). </td></tr><tr><td>0x6</td><td> PWM0 The PWM generator 0 trigger can be configured with the PWM0 Interrupt and Trigger Enable (PWM0INTEN) register (page 1174). </td></tr><tr><td>0x7</td><td> PWM1 The PWM generator 1 trigger can be configured with the PWM1INTEN register (page 1174). </td></tr><tr><td>0x8</td><td> PWM2 The PWM generator 2 trigger can be configured with the PWM2INTEN register (page 1174). </td></tr><tr><td>0x9</td><td> PWM3 The PWM generator 3 trigger can be configured with the PWM3INTEN register (page 1174). </td></tr><tr><td>0xA-0xE</td><td>reserved</td><td></td><td></td><td></td></tr><tr><td>0xF</td><td>Always (continuously sample)</td><td></td><td></td><td></td></tr></table>	Value	Event	0x0	Processor (default) The trigger is initiated by setting the <code>SSn</code> bit in the ADCPSSI register.	0x1	Analog Comparator 0 This trigger is configured by the Analog Comparator Control 0 (ACCTL0) register (page 1127).	0x2	Analog Comparator 1 This trigger is configured by the Analog Comparator Control 1 (ACCTL1) register (page 1127).	0x3	Analog Comparator 2 This trigger is configured by the Analog Comparator Control 2 (ACCTL2) register (page 1127).	0x4	External (GPIO <code>PB4</code>) This trigger is connected to the GPIO interrupt for <code>PB4</code> (see “ADC Trigger Source” on page 410). Note: <code>PB4</code> can be used to trigger the ADC. However, the <code>PB4/AIN10</code> pin cannot be used as both a GPIO and an analog input.	0x5	Timer In addition, the trigger must be enabled with the <code>TnOTE</code> bit in the GPTMCTL register (page 553).	0x6	PWM0 The PWM generator 0 trigger can be configured with the PWM0 Interrupt and Trigger Enable (PWM0INTEN) register (page 1174).	0x7	PWM1 The PWM generator 1 trigger can be configured with the PWM1INTEN register (page 1174).	0x8	PWM2 The PWM generator 2 trigger can be configured with the PWM2INTEN register (page 1174).	0x9	PWM3 The PWM generator 3 trigger can be configured with the PWM3INTEN register (page 1174).	0xA-0xE	reserved				0xF	Always (continuously sample)			
Value	Event																																			
0x0	Processor (default) The trigger is initiated by setting the <code>SSn</code> bit in the ADCPSSI register.																																			
0x1	Analog Comparator 0 This trigger is configured by the Analog Comparator Control 0 (ACCTL0) register (page 1127).																																			
0x2	Analog Comparator 1 This trigger is configured by the Analog Comparator Control 1 (ACCTL1) register (page 1127).																																			
0x3	Analog Comparator 2 This trigger is configured by the Analog Comparator Control 2 (ACCTL2) register (page 1127).																																			
0x4	External (GPIO <code>PB4</code>) This trigger is connected to the GPIO interrupt for <code>PB4</code> (see “ADC Trigger Source” on page 410). Note: <code>PB4</code> can be used to trigger the ADC. However, the <code>PB4/AIN10</code> pin cannot be used as both a GPIO and an analog input.																																			
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0x9	PWM3 The PWM generator 3 trigger can be configured with the PWM3INTEN register (page 1174).																																			
0xA-0xE	reserved																																			
0xF	Always (continuously sample)																																			

Bit/Field	Name	Type	Reset	Description																																
3:0	EM0	R/W	0x0	SS0 Trigger Select This field selects the trigger source for Sample Sequencer 0 The valid configurations for this field are: <table><tr><th>Value</th><th>Event</th></tr><tr><td>0x0</td><td> Processor (default) The trigger is initiated by setting the <code>SSn</code> bit in the ADCPSSI register. </td></tr><tr><td>0x1</td><td> Analog Comparator 0 This trigger is configured by the Analog Comparator Control 0 (ACCTL0) register (page 1127). </td></tr><tr><td>0x2</td><td> Analog Comparator 1 This trigger is configured by the Analog Comparator Control 1 (ACCTL1) register (page 1127). </td></tr><tr><td>0x3</td><td> Analog Comparator 2 This trigger is configured by the Analog Comparator Control 2 (ACCTL2) register (page 1127). </td></tr><tr><td>0x4</td><td> External (GPIO <code>PB4</code>) This trigger is connected to the GPIO interrupt for <code>PB4</code> (see “ADC Trigger Source” on page 410). Note: <code>PB4</code> can be used to trigger the ADC. However, the <code>PB4/AIN10</code> pin cannot be used as both a GPIO and an analog input. </td></tr><tr><td>0x5</td><td> Timer In addition, the trigger must be enabled with the <code>TnOTE</code> bit in the GPTMCTL register (page 553). </td></tr><tr><td>0x6</td><td> PWM0 The PWM generator 0 trigger can be configured with the PWM0 Interrupt and Trigger Enable (PWM0INTEN) register (page 1174). </td></tr><tr><td>0x7</td><td> PWM1 The PWM generator 1 trigger can be configured with the PWM1INTEN register (page 1174). </td></tr><tr><td>0x8</td><td> PWM2 The PWM generator 2 trigger can be configured with the PWM2INTEN register (page 1174). </td></tr><tr><td>0x9</td><td> PWM3 The PWM generator 3 trigger can be configured with the PWM3INTEN register (page 1174). </td></tr><tr><td>0xA-0xE</td><td>reserved</td><td></td><td></td><td></td></tr><tr><td>0xF</td><td>Always (continuously sample)</td><td></td><td></td><td></td></tr></table>	Value	Event	0x0	Processor (default) The trigger is initiated by setting the <code>SSn</code> bit in the ADCPSSI register.	0x1	Analog Comparator 0 This trigger is configured by the Analog Comparator Control 0 (ACCTL0) register (page 1127).	0x2	Analog Comparator 1 This trigger is configured by the Analog Comparator Control 1 (ACCTL1) register (page 1127).	0x3	Analog Comparator 2 This trigger is configured by the Analog Comparator Control 2 (ACCTL2) register (page 1127).	0x4	External (GPIO <code>PB4</code>) This trigger is connected to the GPIO interrupt for <code>PB4</code> (see “ADC Trigger Source” on page 410). Note: <code>PB4</code> can be used to trigger the ADC. However, the <code>PB4/AIN10</code> pin cannot be used as both a GPIO and an analog input.	0x5	Timer In addition, the trigger must be enabled with the <code>TnOTE</code> bit in the GPTMCTL register (page 553).	0x6	PWM0 The PWM generator 0 trigger can be configured with the PWM0 Interrupt and Trigger Enable (PWM0INTEN) register (page 1174).	0x7	PWM1 The PWM generator 1 trigger can be configured with the PWM1INTEN register (page 1174).	0x8	PWM2 The PWM generator 2 trigger can be configured with the PWM2INTEN register (page 1174).	0x9	PWM3 The PWM generator 3 trigger can be configured with the PWM3INTEN register (page 1174).	0xA-0xE	reserved				0xF	Always (continuously sample)			
Value	Event																																			
0x0	Processor (default) The trigger is initiated by setting the <code>SSn</code> bit in the ADCPSSI register.																																			
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0x3	Analog Comparator 2 This trigger is configured by the Analog Comparator Control 2 (ACCTL2) register (page 1127).																																			
0x4	External (GPIO <code>PB4</code>) This trigger is connected to the GPIO interrupt for <code>PB4</code> (see “ADC Trigger Source” on page 410). Note: <code>PB4</code> can be used to trigger the ADC. However, the <code>PB4/AIN10</code> pin cannot be used as both a GPIO and an analog input.																																			
0x5	Timer In addition, the trigger must be enabled with the <code>TnOTE</code> bit in the GPTMCTL register (page 553).																																			
0x6	PWM0 The PWM generator 0 trigger can be configured with the PWM0 Interrupt and Trigger Enable (PWM0INTEN) register (page 1174).																																			
0x7	PWM1 The PWM generator 1 trigger can be configured with the PWM1INTEN register (page 1174).																																			
0x8	PWM2 The PWM generator 2 trigger can be configured with the PWM2INTEN register (page 1174).																																			
0x9	PWM3 The PWM generator 3 trigger can be configured with the PWM3INTEN register (page 1174).																																			
0xA-0xE	reserved																																			
0xF	Always (continuously sample)																																			

Register 7: ADC Underflow Status (ADCUSTAT), offset 0x018

This register indicates underflow conditions in the sample sequencer FIFOs. The corresponding underflow condition is cleared by writing a 1 to the relevant bit position.

ADC Underflow Status (ADCUSTAT)

ADC0 base: 0x4003.8000

ADC1 base: 0x4003.9000

Offset 0x018

Type R/W1C, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved												UV3	UV2	UV1	UV0
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W1C	R/W1C	R/W1C	R/W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:4	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
3	UV3	R/W1C	0	SS3 FIFO Underflow The valid configurations for this field are shown below. This bit is cleared by writing a 1. Value Description 1 The FIFO for the Sample Sequencer has hit an underflow condition, meaning that the FIFO is empty and a read was requested. The problematic read does not move the FIFO pointers, and 0s are returned. 0 The FIFO has not underflowed.
2	UV2	R/W1C	0	SS2 FIFO Underflow The valid configurations are the same as those for the UV3 field. This bit is cleared by writing a 1.
1	UV1	R/W1C	0	SS1 FIFO Underflow The valid configurations are the same as those for the UV3 field. This bit is cleared by writing a 1.
0	UV0	R/W1C	0	SS0 FIFO Underflow The valid configurations are the same as those for the UV3 field. This bit is cleared by writing a 1.

Register 8: ADC Sample Sequencer Priority (ADCSSPRI), offset 0x020

This register sets the priority for each of the sample sequencers. Out of reset, Sequencer 0 has the highest priority, and Sequencer 3 has the lowest priority. When reconfiguring sequence priorities, each sequence must have a unique priority for the ADC to operate properly.

ADC Sample Sequencer Priority (ADCSSPRI)

ADC0 base: 0x4003.8000

ADC1 base: 0x4003.9000

Offset 0x020

Type R/W, reset 0x0000.3210

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved		SS3		reserved		SS2		reserved		SS1		reserved		SS0	
Type	RO	RO	R/W	R/W	RO	RO	R/W	R/W	RO	RO	R/W	R/W	RO	RO	R/W	R/W
Reset	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:14	reserved	RO	0x0000.0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
13:12	SS3	R/W	0x3	SS3 Priority This field contains a binary-encoded value that specifies the priority encoding of Sample Sequencer 3. A priority encoding of 0x0 is highest and 0x3 is lowest. The priorities assigned to the sequencers must be uniquely mapped. The ADC may not operate properly if two or more fields are equal.
11:10	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
9:8	SS2	R/W	0x2	SS2 Priority This field contains a binary-encoded value that specifies the priority encoding of Sample Sequencer 2. A priority encoding of 0x0 is highest and 0x3 is lowest. The priorities assigned to the sequencers must be uniquely mapped. The ADC may not operate properly if two or more fields are equal.
7:6	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
5:4	SS1	R/W	0x1	SS1 Priority This field contains a binary-encoded value that specifies the priority encoding of Sample Sequencer 1. A priority encoding of 0x0 is highest and 0x3 is lowest. The priorities assigned to the sequencers must be uniquely mapped. The ADC may not operate properly if two or more fields are equal.
3:2	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

Bit/Field	Name	Type	Reset	Description
1:0	SS0	R/W	0x0	SS0 Priority This field contains a binary-encoded value that specifies the priority encoding of Sample Sequencer 0. A priority encoding of 0x0 is highest and 0x3 is lowest. The priorities assigned to the sequencers must be uniquely mapped. The ADC may not operate properly if two or more fields are equal.

Register 9: ADC Sample Phase Control (ADCSPC), offset 0x024

This register allows the ADC module to sample at one of 16 different discrete phases from 0.0° through 337.5°. For example, the sample rate could be effectively doubled by sampling a signal using one ADC module configured with the standard sample time and the second ADC module configured with a 180.0° phase lag.

Note: Care should be taken when the PHASE field is non-zero, as the resulting delay in sampling the AIN_x input may result in undesirable system consequences. The time from ADC trigger to sample is increased and could make the response time longer than anticipated. The added latency could have ramifications in the system design. Designers should carefully consider the impact of this delay.

ADC Sample Phase Control (ADCSPC)

ADC0 base: 0x4003.8000
ADC1 base: 0x4003.9000
Offset 0x024
Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved												PHASE			
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:4	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

Bit/Field	Name	Type	Reset	Description																																		
3:0	PHASE	R/W	0x0	Phase Difference This field selects the sample phase difference from the standard sample time. <table><thead><tr><th>Value</th><th>Description</th></tr></thead><tbody><tr><td>0x0</td><td>ADC sample lags by 0.0°</td></tr><tr><td>0x1</td><td>ADC sample lags by 22.5°</td></tr><tr><td>0x2</td><td>ADC sample lags by 45.0°</td></tr><tr><td>0x3</td><td>ADC sample lags by 67.5°</td></tr><tr><td>0x4</td><td>ADC sample lags by 90.0°</td></tr><tr><td>0x5</td><td>ADC sample lags by 112.5°</td></tr><tr><td>0x6</td><td>ADC sample lags by 135.0°</td></tr><tr><td>0x7</td><td>ADC sample lags by 157.5°</td></tr><tr><td>0x8</td><td>ADC sample lags by 180.0°</td></tr><tr><td>0x9</td><td>ADC sample lags by 202.5°</td></tr><tr><td>0xA</td><td>ADC sample lags by 225.0°</td></tr><tr><td>0xB</td><td>ADC sample lags by 247.5°</td></tr><tr><td>0xC</td><td>ADC sample lags by 270.0°</td></tr><tr><td>0xD</td><td>ADC sample lags by 292.5°</td></tr><tr><td>0xE</td><td>ADC sample lags by 315.0°</td></tr><tr><td>0xF</td><td>ADC sample lags by 337.5°</td></tr></tbody></table>	Value	Description	0x0	ADC sample lags by 0.0°	0x1	ADC sample lags by 22.5°	0x2	ADC sample lags by 45.0°	0x3	ADC sample lags by 67.5°	0x4	ADC sample lags by 90.0°	0x5	ADC sample lags by 112.5°	0x6	ADC sample lags by 135.0°	0x7	ADC sample lags by 157.5°	0x8	ADC sample lags by 180.0°	0x9	ADC sample lags by 202.5°	0xA	ADC sample lags by 225.0°	0xB	ADC sample lags by 247.5°	0xC	ADC sample lags by 270.0°	0xD	ADC sample lags by 292.5°	0xE	ADC sample lags by 315.0°	0xF	ADC sample lags by 337.5°
Value	Description																																					
0x0	ADC sample lags by 0.0°																																					
0x1	ADC sample lags by 22.5°																																					
0x2	ADC sample lags by 45.0°																																					
0x3	ADC sample lags by 67.5°																																					
0x4	ADC sample lags by 90.0°																																					
0x5	ADC sample lags by 112.5°																																					
0x6	ADC sample lags by 135.0°																																					
0x7	ADC sample lags by 157.5°																																					
0x8	ADC sample lags by 180.0°																																					
0x9	ADC sample lags by 202.5°																																					
0xA	ADC sample lags by 225.0°																																					
0xB	ADC sample lags by 247.5°																																					
0xC	ADC sample lags by 270.0°																																					
0xD	ADC sample lags by 292.5°																																					
0xE	ADC sample lags by 315.0°																																					
0xF	ADC sample lags by 337.5°																																					

Register 10: ADC Processor Sample Sequence Initiate (ADCPSSI), offset 0x028

This register provides a mechanism for application software to initiate sampling in the sample sequencers. Sample sequences can be initiated individually or in any combination. When multiple sequences are triggered simultaneously, the priority encodings in **ADCSSPRI** dictate execution order.

This register also provides a means to configure and then initiate concurrent sampling on all ADC modules. To do this, the first ADC module should be configured. The **ADCPSSI** register for that module should then be written. The appropriate **SS** bits should be set along with the **SYNCWAIT** bit. Additional ADC modules should then be configured following the same procedure. Once the final ADC module is configured, its **ADCPSSI** register should be written with the appropriate **SS** bits set along with the **GSYNC** bit. All of the ADC modules then begin concurrent sampling according to their configuration.

ADC Processor Sample Sequence Initiate (ADCPSSI)

ADC0 base: 0x4003.8000

ADC1 base: 0x4003.9000

Offset 0x028

Type R/W, reset -

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	GSYNC	reserved				SYNCWAIT	reserved									
Type	R/W	RO	RO	RO	R/W	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved												SS3	SS2	SS1	SS0
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	-	-	-	-

Bit/Field	Name	Type	Reset	Description
31	GSYNC	R/W	0	Global Synchronize
				Value Description
				1 This bit initiates sampling in multiple ADC modules at the same time. Any ADC module that has been initialized by setting an SS_n bit and the SYNCWAIT bit starts sampling once this bit is written.
				0 This bit is cleared once sampling has been initiated.
30:28	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
27	SYNCWAIT	R/W	0	Synchronize Wait
				Value Description
				1 This bit allows the sample sequences to be initiated, but delays sampling until the GSYNC bit is set.
				0 Sampling begins when a sample sequence has been initiated.
26:4	reserved	RO	0x0000.0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

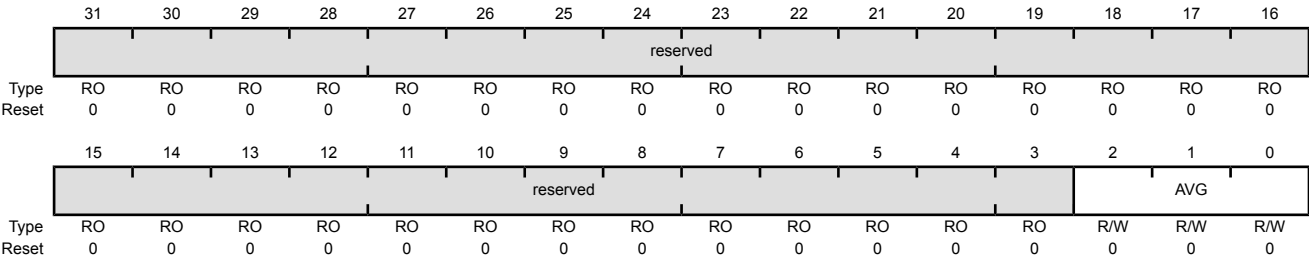
Bit/Field	Name	Type	Reset	Description
3	SS3	WO	-	SS3 Initiate Value Description 1 Begin sampling on Sample Sequencer 3, if the sequencer is enabled in the ADCACTSS register. 0 No effect. Only a write by software is valid; a read of this register returns no meaningful data.
2	SS2	WO	-	SS2 Initiate Value Description 1 Begin sampling on Sample Sequencer 2, if the sequencer is enabled in the ADCACTSS register. 0 No effect. Only a write by software is valid; a read of this register returns no meaningful data.
1	SS1	WO	-	SS1 Initiate Value Description 1 Begin sampling on Sample Sequencer 1, if the sequencer is enabled in the ADCACTSS register. 0 No effect. Only a write by software is valid; a read of this register returns no meaningful data.
0	SS0	WO	-	SS0 Initiate Value Description 1 Begin sampling on Sample Sequencer 0, if the sequencer is enabled in the ADCACTSS register. 0 No effect. Only a write by software is valid; a read of this register returns no meaningful data.

Register 11: ADC Sample Averaging Control (ADCSAC), offset 0x030

This register controls the amount of hardware averaging applied to conversion results. The final conversion result stored in the FIFO is averaged from 2^{AVG} consecutive ADC samples at the specified ADC speed. If AVG is 0, the sample is passed directly through without any averaging. If AVG=6, then 64 consecutive ADC samples are averaged to generate one result in the sequencer FIFO. An AVG=7 provides unpredictable results.

ADC Sample Averaging Control (ADCSAC)

ADC0 base: 0x4003.8000
ADC1 base: 0x4003.9000
Offset 0x030
Type R/W, reset 0x0000.0000



Bit/Field	Name	Type	Reset	Description
31:3	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
2:0	AVG	R/W	0x0	Hardware Averaging Control Specifies the amount of hardware averaging that will be applied to ADC samples. The AVG field can be any value between 0 and 6. Entering a value of 7 creates unpredictable results. Value Description 0x0 No hardware oversampling 0x1 2x hardware oversampling 0x2 4x hardware oversampling 0x3 8x hardware oversampling 0x4 16x hardware oversampling 0x5 32x hardware oversampling 0x6 64x hardware oversampling 0x7 reserved

Register 12: ADC Digital Comparator Interrupt Status and Clear (ADCDCISC), offset 0x034

This register provides status and acknowledgement of digital comparator interrupts. One bit is provided for each comparator.

ADC Digital Comparator Interrupt Status and Clear (ADCDCISC)

ADC0 base: 0x4003.8000

ADC1 base: 0x4003.9000

Offset 0x034

Type R/W1C, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								DCINT7	DCINT6	DCINT5	DCINT4	DCINT3	DCINT2	DCINT1	DCINT0
Type	RO	RO	RO	RO	RO	RO	RO	RO	R/W1C	R/W1C	R/W1C	R/W1C	R/W1C	R/W1C	R/W1C	R/W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7	DCINT7	R/W1C	0	Digital Comparator 7 Interrupt Status and Clear Value Description 1 Digital Comparator 7 has generated an interrupt. 0 No interrupt. This bit is cleared by writing a 1.
6	DCINT6	R/W1C	0	Digital Comparator 6 Interrupt Status and Clear Value Description 1 Digital Comparator 6 has generated an interrupt. 0 No interrupt. This bit is cleared by writing a 1.
5	DCINT5	R/W1C	0	Digital Comparator 5 Interrupt Status and Clear Value Description 1 Digital Comparator 5 has generated an interrupt. 0 No interrupt. This bit is cleared by writing a 1.

Bit/Field	Name	Type	Reset	Description
4	DCINT4	R/W1C	0	Digital Comparator 4 Interrupt Status and Clear Value Description 1 Digital Comparator 4 has generated an interrupt. 0 No interrupt. This bit is cleared by writing a 1.
3	DCINT3	R/W1C	0	Digital Comparator 3 Interrupt Status and Clear Value Description 1 Digital Comparator 3 has generated an interrupt. 0 No interrupt. This bit is cleared by writing a 1.
2	DCINT2	R/W1C	0	Digital Comparator 2 Interrupt Status and Clear Value Description 1 Digital Comparator 2 has generated an interrupt. 0 No interrupt. This bit is cleared by writing a 1.
1	DCINT1	R/W1C	0	Digital Comparator 1 Interrupt Status and Clear Value Description 1 Digital Comparator 1 has generated an interrupt. 0 No interrupt. This bit is cleared by writing a 1.
0	DCINT0	R/W1C	0	Digital Comparator 0 Interrupt Status and Clear Value Description 1 Digital Comparator 0 has generated an interrupt. 0 No interrupt. This bit is cleared by writing a 1.

Register 13: ADC Control (ADCCTL), offset 0x038

This register configures the voltage reference. The voltage reference for the conversion can be the internal 3.0-V reference or an external voltage reference in the range of 2.4 V to 3.06 V.

ADC Control (ADCCTL)

ADC0 base: 0x4003.8000

ADC1 base: 0x4003.9000

Offset 0x038

Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved															VREF
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:1	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
0	VREF	R/W	0	Voltage Reference Select

Value Description

- | | |
|---|---|
| 1 | The external V_{REFA} input is the voltage reference. |
| 0 | The internal reference as the voltage reference. |

Register 14: ADC Sample Sequence Input Multiplexer Select 0 (ADCSSMUX0), offset 0x040

This register defines the analog input configuration for each sample in a sequence executed with Sample Sequencer 0. This register is 32 bits wide and contains information for eight possible samples.

ADC Sample Sequence Input Multiplexer Select 0 (ADCSSMUX0)

ADC0 base: 0x4003.8000

ADC1 base: 0x4003.9000

Offset 0x040

Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MUX7				MUX6				MUX5				MUX4			
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MUX3				MUX2				MUX1				MUX0			
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:28	MUX7	R/W	0x0	8th Sample Input Select The MUX7 field is used during the eighth sample of a sequence executed with the sample sequencer. It specifies which of the analog inputs is sampled for the analog-to-digital conversion. The value set here indicates the corresponding pin, for example, a value of 0x1 indicates the input is AIN1 .
27:24	MUX6	R/W	0x0	7th Sample Input Select The MUX6 field is used during the seventh sample of a sequence executed with the sample sequencer. It specifies which of the analog inputs is sampled for the analog-to-digital conversion.
23:20	MUX5	R/W	0x0	6th Sample Input Select The MUX5 field is used during the sixth sample of a sequence executed with the sample sequencer. It specifies which of the analog inputs is sampled for the analog-to-digital conversion.
19:16	MUX4	R/W	0x0	5th Sample Input Select The MUX4 field is used during the fifth sample of a sequence executed with the sample sequencer. It specifies which of the analog inputs is sampled for the analog-to-digital conversion.
15:12	MUX3	R/W	0x0	4th Sample Input Select The MUX3 field is used during the fourth sample of a sequence executed with the sample sequencer. It specifies which of the analog inputs is sampled for the analog-to-digital conversion.
11:8	MUX2	R/W	0x0	3rd Sample Input Select The MUX2 field is used during the third sample of a sequence executed with the sample sequencer. It specifies which of the analog inputs is sampled for the analog-to-digital conversion.

Bit/Field	Name	Type	Reset	Description
7:4	MUX1	R/W	0x0	2nd Sample Input Select The MUX1 field is used during the second sample of a sequence executed with the sample sequencer. It specifies which of the analog inputs is sampled for the analog-to-digital conversion.
3:0	MUX0	R/W	0x0	1st Sample Input Select The MUX0 field is used during the first sample of a sequence executed with the sample sequencer. It specifies which of the analog inputs is sampled for the analog-to-digital conversion.

Register 15: ADC Sample Sequence Control 0 (ADCSSCTL0), offset 0x044

This register contains the configuration information for each sample for a sequence executed with a sample sequencer. When configuring a sample sequence, the **END** bit must be set for the final sample, whether it be after the first sample, eighth sample, or any sample in between. This register is 32 bits wide and contains information for eight possible samples.

ADC Sample Sequence Control 0 (ADCSSCTL0)

ADC0 base: 0x4003.8000

ADC1 base: 0x4003.9000

Offset 0x044

Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TS7	IE7	END7	D7	TS6	IE6	END6	D6	TS5	IE5	END5	D5	TS4	IE4	END4	D4
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TS3	IE3	END3	D3	TS2	IE2	END2	D2	TS1	IE1	END1	D1	TS0	IE0	END0	D0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31	TS7	R/W	0	8th Sample Temp Sensor Select
				Value Description
				1 The temperature sensor is read during the eighth sample of the sample sequence.
				0 The input pin specified by the ADCSSMUXn register is read during the eighth sample of the sample sequence.
30	IE7	R/W	0	8th Sample Interrupt Enable
				Value Description
				1 The raw interrupt signal (INR0 bit) is asserted at the end of the eighth sample's conversion. If the MASK0 bit in the ADCIM register is set, the interrupt is promoted to the interrupt controller.
				0 The raw interrupt is not asserted to the interrupt controller.
				It is legal to have multiple samples within a sequence generate interrupts.
29	END7	R/W	0	8th Sample is End of Sequence
				Value Description
				1 The eighth sample is the last sample of the sequence.
				0 Another sample in the sequence is the final sample.
				It is possible to end the sequence on any sample position. Software must set an ENDn bit somewhere within the sequence. Samples defined after the sample containing a set ENDn bit are not requested for conversion even though the fields may be non-zero.

Bit/Field	Name	Type	Reset	Description
28	D7	R/W	0	8th Sample Diff Input Select Value Description 1 The analog input is differentially sampled. The corresponding ADCSSMUXn nibble must be set to the pair number "i", where the paired inputs are "2i and 2i+1". 0 The analog inputs are not differentially sampled. Because the temperature sensor does not have a differential option, this bit must not be set when the TS7 bit is set.
27	TS6	R/W	0	7th Sample Temp Sensor Select Same definition as TS7 but used during the seventh sample.
26	IE6	R/W	0	7th Sample Interrupt Enable Same definition as IE7 but used during the seventh sample.
25	END6	R/W	0	7th Sample is End of Sequence Same definition as END7 but used during the seventh sample.
24	D6	R/W	0	7th Sample Diff Input Select Same definition as D7 but used during the seventh sample.
23	TS5	R/W	0	6th Sample Temp Sensor Select Same definition as TS7 but used during the sixth sample.
22	IE5	R/W	0	6th Sample Interrupt Enable Same definition as IE7 but used during the sixth sample.
21	END5	R/W	0	6th Sample is End of Sequence Same definition as END7 but used during the sixth sample.
20	D5	R/W	0	6th Sample Diff Input Select Same definition as D7 but used during the sixth sample.
19	TS4	R/W	0	5th Sample Temp Sensor Select Same definition as TS7 but used during the fifth sample.
18	IE4	R/W	0	5th Sample Interrupt Enable Same definition as IE7 but used during the fifth sample.
17	END4	R/W	0	5th Sample is End of Sequence Same definition as END7 but used during the fifth sample.
16	D4	R/W	0	5th Sample Diff Input Select Same definition as D7 but used during the fifth sample.
15	TS3	R/W	0	4th Sample Temp Sensor Select Same definition as TS7 but used during the fourth sample.
14	IE3	R/W	0	4th Sample Interrupt Enable Same definition as IE7 but used during the fourth sample.

Bit/Field	Name	Type	Reset	Description
13	END3	R/W	0	4th Sample is End of Sequence Same definition as <code>END7</code> but used during the fourth sample.
12	D3	R/W	0	4th Sample Diff Input Select Same definition as <code>D7</code> but used during the fourth sample.
11	TS2	R/W	0	3rd Sample Temp Sensor Select Same definition as <code>TS7</code> but used during the third sample.
10	IE2	R/W	0	3rd Sample Interrupt Enable Same definition as <code>IE7</code> but used during the third sample.
9	END2	R/W	0	3rd Sample is End of Sequence Same definition as <code>END7</code> but used during the third sample.
8	D2	R/W	0	3rd Sample Diff Input Select Same definition as <code>D7</code> but used during the third sample.
7	TS1	R/W	0	2nd Sample Temp Sensor Select Same definition as <code>TS7</code> but used during the second sample.
6	IE1	R/W	0	2nd Sample Interrupt Enable Same definition as <code>IE7</code> but used during the second sample.
5	END1	R/W	0	2nd Sample is End of Sequence Same definition as <code>END7</code> but used during the second sample.
4	D1	R/W	0	2nd Sample Diff Input Select Same definition as <code>D7</code> but used during the second sample.
3	TS0	R/W	0	1st Sample Temp Sensor Select Same definition as <code>TS7</code> but used during the first sample.
2	IE0	R/W	0	1st Sample Interrupt Enable Same definition as <code>IE7</code> but used during the first sample.
1	END0	R/W	0	1st Sample is End of Sequence Same definition as <code>END7</code> but used during the first sample.
0	D0	R/W	0	1st Sample Diff Input Select Same definition as <code>D7</code> but used during the first sample.

Register 16: ADC Sample Sequence Result FIFO 0 (ADCSSFIFO0), offset 0x048

Register 17: ADC Sample Sequence Result FIFO 1 (ADCSSFIFO1), offset 0x068

Register 18: ADC Sample Sequence Result FIFO 2 (ADCSSFIFO2), offset 0x088

Register 19: ADC Sample Sequence Result FIFO 3 (ADCSSFIFO3), offset 0x0A8

Important: This register is read-sensitive. See the register description for details.

This register contains the conversion results for samples collected with the sample sequencer (the **ADCSSFIFO0** register is used for Sample Sequencer 0, **ADCSSFIFO1** for Sequencer 1, **ADCSSFIFO2** for Sequencer 2, and **ADCSSFIFO3** for Sequencer 3). Reads of this register return conversion result data in the order sample 0, sample 1, and so on, until the FIFO is empty. If the FIFO is not properly handled by software, overflow and underflow conditions are registered in the **ADCSTAT** and **ADCUSTAT** registers.

ADC Sample Sequence Result FIFO n (ADCSSFIFO_n)

ADC0 base: 0x4003.8000

ADC1 base: 0x4003.9000

Offset 0x048

Type RO, reset -

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved						DATA									
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	-	-	-	-	-	-	-	-	-	-

Bit/Field	Name	Type	Reset	Description
31:10	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
9:0	DATA	RO	-	Conversion Result Data

Register 20: ADC Sample Sequence FIFO 0 Status (ADCSSFSTAT0), offset 0x04C

Register 21: ADC Sample Sequence FIFO 1 Status (ADCSSFSTAT1), offset 0x06C

Register 22: ADC Sample Sequence FIFO 2 Status (ADCSSFSTAT2), offset 0x08C

Register 23: ADC Sample Sequence FIFO 3 Status (ADCSSFSTAT3), offset 0x0AC

This register provides a window into the sample sequencer, providing full/empty status information as well as the positions of the head and tail pointers. The reset value of 0x100 indicates an empty FIFO with the head and tail pointers both pointing to index 0. The **ADCSSFSTAT0** register provides status on FIFO0, which has 8 entries; **ADCSSFSTAT1** on FIFO1, which has 4 entries; **ADCSSFSTAT2** on FIFO2, which has 4 entries; and **ADCSSFSTAT3** on FIFO3 which has a single entry.

ADC Sample Sequence FIFO 0 Status (ADCSSFSTAT0)

ADC0 base: 0x4003.8000

ADC1 base: 0x4003.9000

Offset 0x04C

Type RO, reset 0x0000.0100

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved			FULL	reserved			EMPTY	HPTR				TPTR			
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:13	reserved	RO	0x0000.0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
12	FULL	RO	0	FIFO Full
				Value Description
				1 The FIFO is currently full.
				0 The FIFO is not currently full.
11:9	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
8	EMPTY	RO	1	FIFO Empty
				Value Description
				1 The FIFO is currently empty.
				0 The FIFO is not currently empty.

Bit/Field	Name	Type	Reset	Description
7:4	HPTR	RO	0x0	FIFO Head Pointer This field contains the current "head" pointer index for the FIFO, that is, the next entry to be written. Valid values are 0x0-0x7 for FIFO0; 0x0-0x3 for FIFO1 and FIFO2; and 0x0 for FIFO3.
3:0	TPTR	RO	0x0	FIFO Tail Pointer This field contains the current "tail" pointer index for the FIFO, that is, the next entry to be read. Valid values are 0x0-0x7 for FIFO0; 0x0-0x3 for FIFO1 and FIFO2; and 0x0 for FIFO3.

Register 24: ADC Sample Sequence 0 Operation (ADCSSOP0), offset 0x050

This register determines whether the sample from the given conversion on Sample Sequence 0 is saved in the Sample Sequence FIFO0 or sent to the digital comparator unit.

ADC Sample Sequence 0 Operation (ADCSSOP0)

ADC0 base: 0x4003.8000

ADC1 base: 0x4003.9000

Offset 0x050

Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved			S7DCOP	reserved			S6DCOP	reserved			S5DCOP	reserved			S4DCOP
Type	RO	RO	RO	R/W	RO	RO	RO	R/W	RO	RO	RO	R/W	RO	RO	RO	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved			S3DCOP	reserved			S2DCOP	reserved			S1DCOP	reserved			S0DCOP
Type	RO	RO	RO	R/W	RO	RO	RO	R/W	RO	RO	RO	R/W	RO	RO	RO	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:29	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
28	S7DCOP	R/W	0	Sample 7 Digital Comparator Operation Value Description 1 The eighth sample is sent to the digital comparator unit specified by the <i>S7DCSEL</i> bit in the ADCSSDC0 register, and the value is not written to the FIFO. 0 The eighth sample is saved in Sample Sequence FIFO0.
27:25	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
24	S6DCOP	R/W	0	Sample 6 Digital Comparator Operation Same definition as <i>S7DCOP</i> but used during the seventh sample.
23:21	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
20	S5DCOP	R/W	0	Sample 5 Digital Comparator Operation Same definition as <i>S7DCOP</i> but used during the sixth sample.
19:17	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
16	S4DCOP	R/W	0	Sample 4 Digital Comparator Operation Same definition as <i>S7DCOP</i> but used during the fifth sample.
15:13	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

Bit/Field	Name	Type	Reset	Description
12	S3DCOP	R/W	0	Sample 3 Digital Comparator Operation Same definition as S7DCOP but used during the fourth sample.
11:9	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
8	S2DCOP	R/W	0	Sample 2 Digital Comparator Operation Same definition as S7DCOP but used during the third sample.
7:5	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
4	S1DCOP	R/W	0	Sample 1 Digital Comparator Operation Same definition as S7DCOP but used during the second sample.
3:1	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
0	S0DCOP	R/W	0	Sample 0 Digital Comparator Operation Same definition as S7DCOP but used during the first sample.

Register 25: ADC Sample Sequence 0 Digital Comparator Select (ADCSSDC0), offset 0x054

This register determines which digital comparator receives the sample from the given conversion on Sample Sequence 0, if the corresponding S_nDCOP bit in the **ADCSSOP0** register is set.

ADC Sample Sequence 0 Digital Comparator Select (ADCSSDC0)

ADC0 base: 0x4003.8000

ADC1 base: 0x4003.9000

Offset 0x054

Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	S7DCSEL				S6DCSEL				S5DCSEL				S4DCSEL			
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	S3DCSEL				S2DCSEL				S1DCSEL				S0DCSEL			
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description																		
31:28	S7DCSEL	R/W	0x0	Sample 7 Digital Comparator Select When the <i>S7DCOP</i> bit in the ADCSSOP0 register is set, this field indicates which digital comparator unit (and its associated set of control registers) receives the eighth sample from Sample Sequencer 0. Note: Values not listed are reserved. <table><tr><th>Value</th><th>Description</th></tr><tr><td>0x0</td><td>Digital Comparator Unit 0 (ADCDCCMP0 and ADCDCCTL0)</td></tr><tr><td>0x1</td><td>Digital Comparator Unit 1 (ADCDCCMP1 and ADCDCCTL1)</td></tr><tr><td>0x2</td><td>Digital Comparator Unit 2 (ADCDCCMP2 and ADCDCCTL2)</td></tr><tr><td>0x3</td><td>Digital Comparator Unit 3 (ADCDCCMP3 and ADCDCCTL3)</td></tr><tr><td>0x4</td><td>Digital Comparator Unit 4 (ADCDCCMP4 and ADCDCCTL4)</td></tr><tr><td>0x5</td><td>Digital Comparator Unit 5 (ADCDCCMP5 and ADCDCCTL5)</td></tr><tr><td>0x6</td><td>Digital Comparator Unit 6 (ADCDCCMP6 and ADCDCCTL6)</td></tr><tr><td>0x7</td><td>Digital Comparator Unit 7 (ADCDCCMP7 and ADCDCCTL7)</td></tr></table>	Value	Description	0x0	Digital Comparator Unit 0 (ADCDCCMP0 and ADCDCCTL0)	0x1	Digital Comparator Unit 1 (ADCDCCMP1 and ADCDCCTL1)	0x2	Digital Comparator Unit 2 (ADCDCCMP2 and ADCDCCTL2)	0x3	Digital Comparator Unit 3 (ADCDCCMP3 and ADCDCCTL3)	0x4	Digital Comparator Unit 4 (ADCDCCMP4 and ADCDCCTL4)	0x5	Digital Comparator Unit 5 (ADCDCCMP5 and ADCDCCTL5)	0x6	Digital Comparator Unit 6 (ADCDCCMP6 and ADCDCCTL6)	0x7	Digital Comparator Unit 7 (ADCDCCMP7 and ADCDCCTL7)
Value	Description																					
0x0	Digital Comparator Unit 0 (ADCDCCMP0 and ADCDCCTL0)																					
0x1	Digital Comparator Unit 1 (ADCDCCMP1 and ADCDCCTL1)																					
0x2	Digital Comparator Unit 2 (ADCDCCMP2 and ADCDCCTL2)																					
0x3	Digital Comparator Unit 3 (ADCDCCMP3 and ADCDCCTL3)																					
0x4	Digital Comparator Unit 4 (ADCDCCMP4 and ADCDCCTL4)																					
0x5	Digital Comparator Unit 5 (ADCDCCMP5 and ADCDCCTL5)																					
0x6	Digital Comparator Unit 6 (ADCDCCMP6 and ADCDCCTL6)																					
0x7	Digital Comparator Unit 7 (ADCDCCMP7 and ADCDCCTL7)																					
27:24	S6DCSEL	R/W	0x0	Sample 6 Digital Comparator Select This field has the same encodings as <i>S7DCSEL</i> but is used during the seventh sample.																		
23:20	S5DCSEL	R/W	0x0	Sample 5 Digital Comparator Select This field has the same encodings as <i>S7DCSEL</i> but is used during the sixth sample.																		
19:16	S4DCSEL	R/W	0x0	Sample 4 Digital Comparator Select This field has the same encodings as <i>S7DCSEL</i> but is used during the fifth sample.																		
15:12	S3DCSEL	R/W	0x0	Sample 3 Digital Comparator Select This field has the same encodings as <i>S7DCSEL</i> but is used during the fourth sample.																		

Bit/Field	Name	Type	Reset	Description
11:8	S2DCSEL	R/W	0x0	Sample 2 Digital Comparator Select This field has the same encodings as S7DCSEL but is used during the third sample.
7:4	S1DCSEL	R/W	0x0	Sample 1 Digital Comparator Select This field has the same encodings as S7DCSEL but is used during the second sample.
3:0	S0DCSEL	R/W	0x0	Sample 0 Digital Comparator Select This field has the same encodings as S7DCSEL but is used during the first sample.

Register 26: ADC Sample Sequence Input Multiplexer Select 1 (ADCSSMUX1), offset 0x060**Register 27: ADC Sample Sequence Input Multiplexer Select 2 (ADCSSMUX2), offset 0x080**

This register defines the analog input configuration for each sample in a sequence executed with Sample Sequencer 1 or 2. These registers are 16 bits wide and contain information for four possible samples. See the **ADCSSMUX0** register on page 652 for detailed bit descriptions. The **ADCSSMUX1** register affects Sample Sequencer 1 and the **ADCSSMUX2** register affects Sample Sequencer 2.

ADC Sample Sequence Input Multiplexer Select 1 (ADCSSMUX1)

ADC0 base: 0x4003.8000

ADC1 base: 0x4003.9000

Offset 0x060

Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MUX3				MUX2				MUX1				MUX0			
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:16	reserved	RO	0x0000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
15:12	MUX3	R/W	0x0	4th Sample Input Select
11:8	MUX2	R/W	0x0	3rd Sample Input Select
7:4	MUX1	R/W	0x0	2nd Sample Input Select
3:0	MUX0	R/W	0x0	1st Sample Input Select

Register 28: ADC Sample Sequence Control 1 (ADCSSCTL1), offset 0x064**Register 29: ADC Sample Sequence Control 2 (ADCSSCTL2), offset 0x084**

These registers contain the configuration information for each sample for a sequence executed with Sample Sequencer 1 or 2. When configuring a sample sequence, the **END** bit must be set for the final sample, whether it be after the first sample, fourth sample, or any sample in between. These registers are 16-bits wide and contain information for four possible samples. See the **ADCSSCTL0** register on page 654 for detailed bit descriptions. The **ADCSSCTL1** register configures Sample Sequencer 1 and the **ADCSSCTL2** register configures Sample Sequencer 2.

ADC Sample Sequence Control 1 (ADCSSCTL1)

ADC0 base: 0x4003.8000

ADC1 base: 0x4003.9000

Offset 0x064

Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TS3	IE3	END3	D3	TS2	IE2	END2	D2	TS1	IE1	END1	D1	TS0	IE0	END0	D0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:16	reserved	RO	0x0000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
15	TS3	R/W	0	4th Sample Temp Sensor Select Same definition as TS7 but used during the fourth sample.
14	IE3	R/W	0	4th Sample Interrupt Enable Same definition as IE7 but used during the fourth sample.
13	END3	R/W	0	4th Sample is End of Sequence Same definition as END7 but used during the fourth sample.
12	D3	R/W	0	4th Sample Diff Input Select Same definition as D7 but used during the fourth sample.
11	TS2	R/W	0	3rd Sample Temp Sensor Select Same definition as TS7 but used during the third sample.
10	IE2	R/W	0	3rd Sample Interrupt Enable Same definition as IE7 but used during the third sample.
9	END2	R/W	0	3rd Sample is End of Sequence Same definition as END7 but used during the third sample.
8	D2	R/W	0	3rd Sample Diff Input Select Same definition as D7 but used during the third sample.

Bit/Field	Name	Type	Reset	Description
7	TS1	R/W	0	2nd Sample Temp Sensor Select Same definition as TS7 but used during the second sample.
6	IE1	R/W	0	2nd Sample Interrupt Enable Same definition as IE7 but used during the second sample.
5	END1	R/W	0	2nd Sample is End of Sequence Same definition as END7 but used during the second sample.
4	D1	R/W	0	2nd Sample Diff Input Select Same definition as D7 but used during the second sample.
3	TS0	R/W	0	1st Sample Temp Sensor Select Same definition as TS7 but used during the first sample.
2	IE0	R/W	0	1st Sample Interrupt Enable Same definition as IE7 but used during the first sample.
1	END0	R/W	0	1st Sample is End of Sequence Same definition as END7 but used during the first sample.
0	D0	R/W	0	1st Sample Diff Input Select Same definition as D7 but used during the first sample.

Register 30: ADC Sample Sequence 1 Operation (ADCSSOP1), offset 0x070**Register 31: ADC Sample Sequence 2 Operation (ADCSSOP2), offset 0x090**

This register determines whether the sample from the given conversion on Sample Sequence n is saved in the Sample Sequence n FIFO or sent to the digital comparator unit. The **ADCSSOP1** register controls Sample Sequencer 1 and the **ADCSSOP2** register controls Sample Sequencer 2.

ADC Sample Sequence 1 Operation (ADCSSOP1)

ADC0 base: 0x4003.8000

ADC1 base: 0x4003.9000

Offset 0x070

Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved			S3DCOP	reserved			S2DCOP	reserved			S1DCOP	reserved			S0DCOP
Type	RO	RO	RO	R/W	RO	RO	RO	R/W	RO	RO	RO	R/W	RO	RO	RO	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:13	reserved	RO	0x0000.0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
12	S3DCOP	R/W	0	Sample 3 Digital Comparator Operation
				Value Description
			1	The fourth sample is sent to the digital comparator unit specified by the S3DCSEL bit in the ADCSSDC0n register, and the value is not written to the FIFO.
			0	The fourth sample is saved in Sample Sequence FIFO.
11:9	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
8	S2DCOP	R/W	0	Sample 2 Digital Comparator Operation
				Same definition as S3DCOP but used during the third sample.
7:5	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
4	S1DCOP	R/W	0	Sample 1 Digital Comparator Operation
				Same definition as S3DCOP but used during the second sample.
3:1	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
0	S0DCOP	R/W	0	Sample 0 Digital Comparator Operation
				Same definition as S3DCOP but used during the first sample.

Register 32: ADC Sample Sequence 1 Digital Comparator Select (ADCSSDC1), offset 0x074**Register 33: ADC Sample Sequence 2 Digital Comparator Select (ADCSSDC2), offset 0x094**

These registers determine which digital comparator receives the sample from the given conversion on Sample Sequence n if the corresponding S_nDCOP bit in the **ADCSSOPn** register is set. The **ADCSSDC1** register controls the selection for Sample Sequencer 1 and the **ADCSSDC2** register controls the selection for Sample Sequencer 2.

ADC Sample Sequence 1 Digital Comparator Select (ADCSSDC1)

ADC0 base: 0x4003.8000
 ADC1 base: 0x4003.9000
 Offset 0x074
 Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	S3DCSEL				S2DCSEL				S1DCSEL				S0DCSEL			
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description																		
31:16	reserved	RO	0x0000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.																		
15:12	S3DCSEL	R/W	0x0	Sample 3 Digital Comparator Select When the <i>S3DCOP</i> bit in the ADCSSOPn register is set, this field indicates which digital comparator unit (and its associated set of control registers) receives the eighth sample from Sample Sequencer n. Note: Values not listed are reserved. <table><thead><tr><th>Value</th><th>Description</th></tr></thead><tbody><tr><td>0x0</td><td>Digital Comparator Unit 0 (ADCDCCMP0 and ADCCCTL0)</td></tr><tr><td>0x1</td><td>Digital Comparator Unit 1 (ADCDCCMP1 and ADCCCTL1)</td></tr><tr><td>0x2</td><td>Digital Comparator Unit 2 (ADCDCCMP2 and ADCCCTL2)</td></tr><tr><td>0x3</td><td>Digital Comparator Unit 3 (ADCDCCMP3 and ADCCCTL3)</td></tr><tr><td>0x4</td><td>Digital Comparator Unit 4 (ADCDCCMP4 and ADCCCTL4)</td></tr><tr><td>0x5</td><td>Digital Comparator Unit 5 (ADCDCCMP5 and ADCCCTL5)</td></tr><tr><td>0x6</td><td>Digital Comparator Unit 6 (ADCDCCMP6 and ADCCCTL6)</td></tr><tr><td>0x7</td><td>Digital Comparator Unit 7 (ADCDCCMP7 and ADCCCTL7)</td></tr></tbody></table>	Value	Description	0x0	Digital Comparator Unit 0 (ADCDCCMP0 and ADCCCTL0)	0x1	Digital Comparator Unit 1 (ADCDCCMP1 and ADCCCTL1)	0x2	Digital Comparator Unit 2 (ADCDCCMP2 and ADCCCTL2)	0x3	Digital Comparator Unit 3 (ADCDCCMP3 and ADCCCTL3)	0x4	Digital Comparator Unit 4 (ADCDCCMP4 and ADCCCTL4)	0x5	Digital Comparator Unit 5 (ADCDCCMP5 and ADCCCTL5)	0x6	Digital Comparator Unit 6 (ADCDCCMP6 and ADCCCTL6)	0x7	Digital Comparator Unit 7 (ADCDCCMP7 and ADCCCTL7)
Value	Description																					
0x0	Digital Comparator Unit 0 (ADCDCCMP0 and ADCCCTL0)																					
0x1	Digital Comparator Unit 1 (ADCDCCMP1 and ADCCCTL1)																					
0x2	Digital Comparator Unit 2 (ADCDCCMP2 and ADCCCTL2)																					
0x3	Digital Comparator Unit 3 (ADCDCCMP3 and ADCCCTL3)																					
0x4	Digital Comparator Unit 4 (ADCDCCMP4 and ADCCCTL4)																					
0x5	Digital Comparator Unit 5 (ADCDCCMP5 and ADCCCTL5)																					
0x6	Digital Comparator Unit 6 (ADCDCCMP6 and ADCCCTL6)																					
0x7	Digital Comparator Unit 7 (ADCDCCMP7 and ADCCCTL7)																					
11:8	S2DCSEL	R/W	0x0	Sample 2 Digital Comparator Select This field has the same encodings as <i>S3DCSEL</i> but is used during the third sample.																		

Bit/Field	Name	Type	Reset	Description
7:4	S1DCSEL	R/W	0x0	Sample 1 Digital Comparator Select This field has the same encodings as S3DCSEL but is used during the second sample.
3:0	S0DCSEL	R/W	0x0	Sample 0 Digital Comparator Select This field has the same encodings as S3DCSEL but is used during the first sample.

Register 34: ADC Sample Sequence Input Multiplexer Select 3 (ADCSSMUX3), offset 0x0A0

This register defines the analog input configuration for the sample executed with Sample Sequencer 3. This register is 4 bits wide and contains information for one possible sample. See the **ADCSSMUX0** register on page 652 for detailed bit descriptions.

ADC Sample Sequence Input Multiplexer Select 3 (ADCSSMUX3)

ADC0 base: 0x4003.8000
ADC1 base: 0x4003.9000
Offset 0x0A0
Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved												MUX0			
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:4	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
3:0	MUX0	R/W	0	1st Sample Input Select

Register 35: ADC Sample Sequence Control 3 (ADCSSCTL3), offset 0x0A4

This register contains the configuration information for a sample executed with Sample Sequencer 3. The **END0** bit is always set as this sequencer can execute only one sample. This register is 4 bits wide and contains information for one possible sample. See the **ADCSSCTL0** register on page 654 for detailed bit descriptions.

ADC Sample Sequence Control 3 (ADCSSCTL3)

ADC0 base: 0x4003.8000

ADC1 base: 0x4003.9000

Offset 0x0A4

Type R/W, reset 0x0000.0002

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved												TS0	IE0	END0	D0
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bit/Field	Name	Type	Reset	Description
31:4	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
3	TS0	R/W	0	1st Sample Temp Sensor Select Same definition as TS7 but used during the first sample.
2	IE0	R/W	0	1st Sample Interrupt Enable Same definition as IE7 but used during the first sample.
1	END0	R/W	1	1st Sample is End of Sequence Same definition as END7 but used during the first sample. Because this sequencer has only one entry, this bit must be set.
0	D0	R/W	0	1st Sample Diff Input Select Same definition as D7 but used during the first sample.

Register 36: ADC Sample Sequence 3 Operation (ADCSSOP3), offset 0x0B0

This register determines whether the sample from the given conversion on Sample Sequence 3 is saved in the Sample Sequence 3 FIFO or sent to the digital comparator unit.

ADC Sample Sequence 3 Operation (ADCSSOP3)

ADC0 base: 0x4003.8000

ADC1 base: 0x4003.9000

Offset 0x0B0

Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved															S0DCOP
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:1	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
0	S0DCOP	R/W	0	Sample 0 Digital Comparator Operation

Value Description

- | | |
|---|---|
| 1 | The sample is sent to the digital comparator unit specified by the S0DCSEL bit in the ADCSSDC03 register, and the value is not written to the FIFO. |
| 0 | The sample is saved in Sample Sequence FIFO3. |

Register 37: ADC Sample Sequence 3 Digital Comparator Select (ADCSSDC3), offset 0x0B4

This register determines which digital comparator receives the sample from the given conversion on Sample Sequence 3 if the corresponding S_nDCOP bit in the **ADCSSOP3** register is set.

ADC Sample Sequence 3 Digital Comparator Select (ADCSSDC3)

ADC0 base: 0x4003.8000
 ADC1 base: 0x4003.9000
 Offset 0x0B4
 Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved												S0DCSEL			
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:4	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
3:0	S0DCSEL	R/W	0x0	Sample 0 Digital Comparator Select When the $S0DCOP$ bit in the ADCSSOP3 register is set, this field indicates which digital comparator unit (and its associated set of control registers) receives the sample from Sample Sequencer 3.

Note: Values not listed are reserved.

Value Description

0x0	Digital Comparator Unit 0 (ADCDCOMP0 and ADCCCTL0)
0x1	Digital Comparator Unit 1 (ADCDCOMP1 and ADCCCTL1)
0x2	Digital Comparator Unit 2 (ADCDCOMP2 and ADCCCTL2)
0x3	Digital Comparator Unit 3 (ADCDCOMP3 and ADCCCTL3)
0x4	Digital Comparator Unit 4 (ADCDCOMP4 and ADCCCTL4)
0x5	Digital Comparator Unit 5 (ADCDCOMP5 and ADCCCTL5)
0x6	Digital Comparator Unit 6 (ADCDCOMP6 and ADCCCTL6)
0x7	Digital Comparator Unit 7 (ADCDCOMP7 and ADCCCTL7)

Register 38: ADC Digital Comparator Reset Initial Conditions (ADCDCRIC), offset 0xD00

This register provides the ability to reset any of the digital comparator interrupt or trigger functions back to their initial conditions. Resetting these functions ensures that the data that is being used by the interrupt and trigger functions in the digital comparator unit is not stale.

ADC Digital Comparator Reset Initial Conditions (ADCDCRIC)

ADC0 base: 0x4003.8000

ADC1 base: 0x4003.9000

Offset 0xD00

Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved								DCTRIG7	DCTRIG6	DCTRIG5	DCTRIG4	DCTRIG3	DCTRIG2	DCTRIG1	DCTRIG0
Type	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								DCINT7	DCINT6	DCINT5	DCINT4	DCINT3	DCINT2	DCINT1	DCINT0
Type	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:24	reserved	RO	0x00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
23	DCTRIG7	R/W	0	Digital Comparator Trigger 7 Value Description 1 Resets the Digital Comparator 7 trigger unit to its initial conditions. 0 No effect. When the trigger has been cleared, this bit is automatically cleared. Because the digital comparators use the current and previous ADC conversion values to determine when to assert the trigger, it is important to reset the digital comparator to initial conditions when starting a new sequence so that stale data is not used. After setting this bit, software should wait until the bit clears before continuing.
22	DCTRIG6	R/W	0	Digital Comparator Trigger 6 Value Description 1 Resets the Digital Comparator 6 trigger unit to its initial conditions. 0 No effect. When the trigger has been cleared, this bit is automatically cleared. Because the digital comparators use the current and previous ADC conversion values to determine when to assert the trigger, it is important to reset the digital comparator to initial conditions when starting a new sequence so that stale data is not used.

Bit/Field	Name	Type	Reset	Description
21	DCTRIG5	R/W	0	Digital Comparator Trigger 5 Value Description 1 Resets the Digital Comparator 5 trigger unit to its initial conditions. 0 No effect. When the trigger has been cleared, this bit is automatically cleared. Because the digital comparators use the current and previous ADC conversion values to determine when to assert the trigger, it is important to reset the digital comparator to initial conditions when starting a new sequence so that stale data is not used.
20	DCTRIG4	R/W	0	Digital Comparator Trigger 4 Value Description 1 Resets the Digital Comparator 4 trigger unit to its initial conditions. 0 No effect. When the trigger has been cleared, this bit is automatically cleared. Because the digital comparators use the current and previous ADC conversion values to determine when to assert the trigger, it is important to reset the digital comparator to initial conditions when starting a new sequence so that stale data is not used.
19	DCTRIG3	R/W	0	Digital Comparator Trigger 3 Value Description 1 Resets the Digital Comparator 3 trigger unit to its initial conditions. 0 No effect. When the trigger has been cleared, this bit is automatically cleared. Because the digital comparators use the current and previous ADC conversion values to determine when to assert the trigger, it is important to reset the digital comparator to initial conditions when starting a new sequence so that stale data is not used.
18	DCTRIG2	R/W	0	Digital Comparator Trigger 2 Value Description 1 Resets the Digital Comparator 2 trigger unit to its initial conditions. 0 No effect. When the trigger has been cleared, this bit is automatically cleared. Because the digital comparators use the current and previous ADC conversion values to determine when to assert the trigger, it is important to reset the digital comparator to initial conditions when starting a new sequence so that stale data is not used.

Bit/Field	Name	Type	Reset	Description
17	DCTRIG1	R/W	0	Digital Comparator Trigger 1 Value Description 1 Resets the Digital Comparator 1 trigger unit to its initial conditions. 0 No effect. When the trigger has been cleared, this bit is automatically cleared. Because the digital comparators use the current and previous ADC conversion values to determine when to assert the trigger, it is important to reset the digital comparator to initial conditions when starting a new sequence so that stale data is not used.
16	DCTRIG0	R/W	0	Digital Comparator Trigger 0 Value Description 1 Resets the Digital Comparator 0 trigger unit to its initial conditions. 0 No effect. When the trigger has been cleared, this bit is automatically cleared. Because the digital comparators use the current and previous ADC conversion values to determine when to assert the trigger, it is important to reset the digital comparator to initial conditions when starting a new sequence so that stale data is not used.
15:8	reserved	RO	0x00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7	DCINT7	R/W	0	Digital Comparator Interrupt 7 Value Description 1 Resets the Digital Comparator 7 interrupt unit to its initial conditions. 0 No effect. When the interrupt has been cleared, this bit is automatically cleared. Because the digital comparators use the current and previous ADC conversion values to determine when to assert the interrupt, it is important to reset the digital comparator to initial conditions when starting a new sequence so that stale data is not used.
6	DCINT6	R/W	0	Digital Comparator Interrupt 6 Value Description 1 Resets the Digital Comparator 6 interrupt unit to its initial conditions. 0 No effect. When the interrupt has been cleared, this bit is automatically cleared. Because the digital comparators use the current and previous ADC conversion values to determine when to assert the interrupt, it is important to reset the digital comparator to initial conditions when starting a new sequence so that stale data is not used.

Bit/Field	Name	Type	Reset	Description
5	DCINT5	R/W	0	Digital Comparator Interrupt 5 Value Description 1 Resets the Digital Comparator 5 interrupt unit to its initial conditions. 0 No effect. When the interrupt has been cleared, this bit is automatically cleared. Because the digital comparators use the current and previous ADC conversion values to determine when to assert the interrupt, it is important to reset the digital comparator to initial conditions when starting a new sequence so that stale data is not used.
4	DCINT4	R/W	0	Digital Comparator Interrupt 4 Value Description 1 Resets the Digital Comparator 4 interrupt unit to its initial conditions. 0 No effect. When the interrupt has been cleared, this bit is automatically cleared. Because the digital comparators use the current and previous ADC conversion values to determine when to assert the interrupt, it is important to reset the digital comparator to initial conditions when starting a new sequence so that stale data is not used.
3	DCINT3	R/W	0	Digital Comparator Interrupt 3 Value Description 1 Resets the Digital Comparator 3 interrupt unit to its initial conditions. 0 No effect. When the interrupt has been cleared, this bit is automatically cleared. Because the digital comparators use the current and previous ADC conversion values to determine when to assert the interrupt, it is important to reset the digital comparator to initial conditions when starting a new sequence so that stale data is not used.
2	DCINT2	R/W	0	Digital Comparator Interrupt 2 Value Description 1 Resets the Digital Comparator 2 interrupt unit to its initial conditions. 0 No effect. When the interrupt has been cleared, this bit is automatically cleared. Because the digital comparators use the current and previous ADC conversion values to determine when to assert the interrupt, it is important to reset the digital comparator to initial conditions when starting a new sequence so that stale data is not used.

Bit/Field	Name	Type	Reset	Description
1	DCINT1	R/W	0	Digital Comparator Interrupt 1 Value Description 1 Resets the Digital Comparator 1 interrupt unit to its initial conditions. 0 No effect. When the interrupt has been cleared, this bit is automatically cleared. Because the digital comparators use the current and previous ADC conversion values to determine when to assert the interrupt, it is important to reset the digital comparator to initial conditions when starting a new sequence so that stale data is not used.
0	DCINT0	R/W	0	Digital Comparator Interrupt 0 Value Description 1 Resets the Digital Comparator 0 interrupt unit to its initial conditions. 0 No effect. When the interrupt has been cleared, this bit is automatically cleared. Because the digital comparators use the current and previous ADC conversion values to determine when to assert the interrupt, it is important to reset the digital comparator to initial conditions when starting a new sequence so that stale data is not used.

Register 39: ADC Digital Comparator Control 0 (ADCDCTL0), offset 0xE00

Register 40: ADC Digital Comparator Control 1 (ADCDCTL1), offset 0xE04

Register 41: ADC Digital Comparator Control 2 (ADCDCTL2), offset 0xE08

Register 42: ADC Digital Comparator Control 3 (ADCDCTL3), offset 0xE0C

Register 43: ADC Digital Comparator Control 4 (ADCDCTL4), offset 0xE10

Register 44: ADC Digital Comparator Control 5 (ADCDCTL5), offset 0xE14

Register 45: ADC Digital Comparator Control 6 (ADCDCTL6), offset 0xE18

Register 46: ADC Digital Comparator Control 7 (ADCDCTL7), offset 0xE1C

This register provides the comparison encodings that generate an interrupt and/or PWM trigger. See "Interrupt/ADC-Trigger Selector" on page 1137 for more information on using the ADC digital comparators to trigger a PWM generator.

ADC Digital Comparator Control 0 (ADCDCTL0)

ADC0 base: 0x4003.8000

ADC1 base: 0x4003.9000

Offset 0xE00

Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved			CTE	CTC		CTM		reserved			CIE	CIC		CIM	
Type	RO	RO	RO	R/W	R/W	R/W	R/W	R/W	RO	RO	RO	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:13	reserved	RO	0x0000.0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
12	CTE	R/W	0	Comparison Trigger Enable

Value Description

- | | |
|---|---|
| 1 | Enables the trigger function state machine. The ADC conversion data is used to determine if a trigger should be generated according to the programming of the CTC and CTM fields. |
| 0 | Disables the trigger function state machine. ADC conversion data is ignored by the trigger function. |

Bit/Field	Name	Type	Reset	Description										
11:10	CTC	R/W	0x0	Comparison Trigger Condition This field specifies the operational region in which a trigger is generated when the ADC conversion data is compared against the values of <code>COMP0</code> and <code>COMP1</code>. The <code>COMP0</code> and <code>COMP1</code> fields are defined in the ADCDCCMPx registers. <table><tr><th>Value</th><th>Description</th></tr><tr><td>0x0</td><td>Low Band $\text{ADC Data} < \text{COMP0} \leq \text{COMP1}$</td></tr><tr><td>0x1</td><td>Mid Band $\text{COMP0} \leq \text{ADC Data} < \text{COMP1}$</td></tr><tr><td>0x2</td><td>reserved</td></tr><tr><td>0x3</td><td>High Band $\text{COMP0} \leq \text{COMP1} \leq \text{ADC Data}$</td></tr></table>	Value	Description	0x0	Low Band $\text{ADC Data} < \text{COMP0} \leq \text{COMP1}$	0x1	Mid Band $\text{COMP0} \leq \text{ADC Data} < \text{COMP1}$	0x2	reserved	0x3	High Band $\text{COMP0} \leq \text{COMP1} \leq \text{ADC Data}$
Value	Description													
0x0	Low Band $\text{ADC Data} < \text{COMP0} \leq \text{COMP1}$													
0x1	Mid Band $\text{COMP0} \leq \text{ADC Data} < \text{COMP1}$													
0x2	reserved													
0x3	High Band $\text{COMP0} \leq \text{COMP1} \leq \text{ADC Data}$													
9:8	CTM	R/W	0x0	Comparison Trigger Mode This field specifies the mode by which the trigger comparison is made. <table><tr><th>Value</th><th>Description</th></tr><tr><td>0x0</td><td>Always This mode generates a trigger every time the ADC conversion data falls within the selected operational region.</td></tr><tr><td>0x1</td><td>Once This mode generates a trigger the first time that the ADC conversion data enters the selected operational region.</td></tr><tr><td>0x2</td><td>Hysteresis Always This mode generates a trigger when the ADC conversion data falls within the selected operational region and continues to generate the trigger until the hysteresis condition is cleared by entering the opposite operational region. Note that the hysteresis modes are only defined for <code>CTC</code> encodings of 0x0 and 0x3.</td></tr><tr><td>0x3</td><td>Hysteresis Once This mode generates a trigger the first time that the ADC conversion data falls within the selected operational region. No additional triggers are generated until the hysteresis condition is cleared by entering the opposite operational region. Note that the hysteresis modes are only defined for <code>CTC</code> encodings of 0x0 and 0x3.</td></tr></table>	Value	Description	0x0	Always This mode generates a trigger every time the ADC conversion data falls within the selected operational region.	0x1	Once This mode generates a trigger the first time that the ADC conversion data enters the selected operational region.	0x2	Hysteresis Always This mode generates a trigger when the ADC conversion data falls within the selected operational region and continues to generate the trigger until the hysteresis condition is cleared by entering the opposite operational region. Note that the hysteresis modes are only defined for <code>CTC</code> encodings of 0x0 and 0x3.	0x3	Hysteresis Once This mode generates a trigger the first time that the ADC conversion data falls within the selected operational region. No additional triggers are generated until the hysteresis condition is cleared by entering the opposite operational region. Note that the hysteresis modes are only defined for <code>CTC</code> encodings of 0x0 and 0x3.
Value	Description													
0x0	Always This mode generates a trigger every time the ADC conversion data falls within the selected operational region.													
0x1	Once This mode generates a trigger the first time that the ADC conversion data enters the selected operational region.													
0x2	Hysteresis Always This mode generates a trigger when the ADC conversion data falls within the selected operational region and continues to generate the trigger until the hysteresis condition is cleared by entering the opposite operational region. Note that the hysteresis modes are only defined for <code>CTC</code> encodings of 0x0 and 0x3.													
0x3	Hysteresis Once This mode generates a trigger the first time that the ADC conversion data falls within the selected operational region. No additional triggers are generated until the hysteresis condition is cleared by entering the opposite operational region. Note that the hysteresis modes are only defined for <code>CTC</code> encodings of 0x0 and 0x3.													
7:5	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.										

Bit/Field	Name	Type	Reset	Description
4	CIE	R/W	0	Comparison Interrupt Enable Value Description 1 Enables the comparison interrupt. The ADC conversion data is used to determine if an interrupt should be generated according to the programming of the CIE and CIM fields. 0 Disables the comparison interrupt. ADC conversion data has no effect on interrupt generation.
3:2	CIC	R/W	0x0	Comparison Interrupt Condition This field specifies the operational region in which an interrupt is generated when the ADC conversion data is compared against the values of COMP0 and COMP1. The COMP0 and COMP1 fields are defined in the ADCDCCMPx registers. Value Description 0x0 Low Band $ADC\ Data < COMP0 \leq COMP1$ 0x1 Mid Band $COMP0 \leq ADC\ Data < COMP1$ 0x2 reserved 0x3 High Band $COMP0 < COMP1 \leq ADC\ Data$
1:0	CIM	R/W	0x0	Comparison Interrupt Mode This field specifies the mode by which the interrupt comparison is made. Value Description 0x0 Always This mode generates an interrupt every time the ADC conversion data falls within the selected operational region. 0x1 Once This mode generates an interrupt the first time that the ADC conversion data enters the selected operational region. 0x2 Hysteresis Always This mode generates an interrupt when the ADC conversion data falls within the selected operational region and continues to generate the interrupt until the hysteresis condition is cleared by entering the opposite operational region. Note that the hysteresis modes are only defined for CTC encodings of 0x0 and 0x3. 0x3 Hysteresis Once This mode generates an interrupt the first time that the ADC conversion data falls within the selected operational region. No additional interrupts are generated until the hysteresis condition is cleared by entering the opposite operational region. Note that the hysteresis modes are only defined for CTC encodings of 0x0 and 0x3.

Register 47: ADC Digital Comparator Range 0 (ADCDCCMP0), offset 0xE40

Register 48: ADC Digital Comparator Range 1 (ADCDCCMP1), offset 0xE44

Register 49: ADC Digital Comparator Range 2 (ADCDCCMP2), offset 0xE48

Register 50: ADC Digital Comparator Range 3 (ADCDCCMP3), offset 0xE4C

Register 51: ADC Digital Comparator Range 4 (ADCDCCMP4), offset 0xE50

Register 52: ADC Digital Comparator Range 5 (ADCDCCMP5), offset 0xE54

Register 53: ADC Digital Comparator Range 6 (ADCDCCMP6), offset 0xE58

Register 54: ADC Digital Comparator Range 7 (ADCDCCMP7), offset 0xE5C

This register defines the comparison values that are used to determine if the ADC conversion data falls in the appropriate operating region.

Note: The value in the `COMP1` field must be greater than or equal to the value in the `COMP0` field or unexpected results can occur.

ADC Digital Comparator Range 0 (ADCDCCMP0)

ADC0 base: 0x4003.8000

ADC1 base: 0x4003.9000

Offset 0xE40

Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved						COMP1									
Type	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved						COMP0									
Type	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:26	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
25:16	COMP1	R/W	0x000	Compare 1 The value in this field is compared against the ADC conversion data. The result of the comparison is used to determine if the data lies within the high-band region. Note that the value of <code>COMP1</code> must be greater than or equal to the value of <code>COMP0</code>.
15:10	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
9:0	COMP0	R/W	0x000	Compare 0 The value in this field is compared against the ADC conversion data. The result of the comparison is used to determine if the data lies within the low-band region.