2N7000
2N7002

N-channel 60 V, 1.8 Ω, 0.35 A, SOT23-3L, TO-92
STripFET™ Power MOSFET

Features

Type	V_{DSS}	$R_{DS(on)}$ max	I_D
2N7000	60 V	< 5 Ω(@10V)	0.35 A
2N7002	60 V	< 5 Ω(@10V)	0.20 A

- Low Q_g
- Low threshold drive

Application

- Switching applications

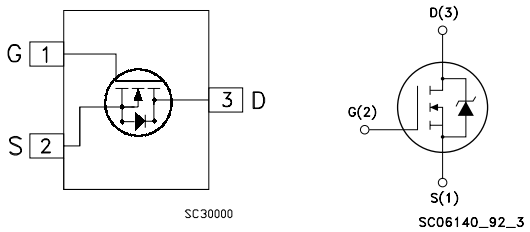
Description

This Power MOSFET is the second generation of STMicroelectronics unique “single feature size” strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.



SOT23-3L TO-92

Figure 1. Internal schematic diagram



SOT23-3L TO-92

Table 1. Device summary

Order codes	Marking	Package	Packaging
2N7000	2N7000G	TO-92	Bulk
2N7002	ST2N	SOT23-3L	Tape and reel

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-92	SOT23-3L	
V_{DS}	Drain-source voltage (V_{GS} = 0)	60		V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 kΩ)	60		V
V_{GS}	Gate- source voltage	± 18		V
I_D	Drain current (continuous) at T_C = 25 °C	0.35	0.20	A
I_{DM} (1)	Drain current (pulsed)	1.4	1	A
P_{TOT}	Total dissipation at T_C = 25 °C	1	0.35	W

1. Pulse width limited by safe operating area

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		TO-92	SOT23-3L	
Rthj-amb	Thermal resistance junction-ambient max	125	357.1 (1)	°C/W
T_J	Operating junction temperature	- 55 to 150		°C
T_{stg}	Storage temperature			

1. When mounted on 1inch² FR-4, 2 Oz copper board.

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS} =0	60			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = max rating V_{DS} = max rating, T_C = 125 °C			1 10	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 18 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	1	2.1	3	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 0.5 A V_{GS} = 4.5 V, I_D = 0.5 A		1.8 2	5 5.3	Ω Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 10 V , I_D = 0.5 A		0.6		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0		43 20 6		pF pF pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} = 30 V, I_D = 0.5 A R_G = 4.7 Ω V_{GS} = 4.5 V (see *Figure 16*)		5 15 7 8		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 30 V, I_D = 1 A, V_{GS} = 5 V (see *Figure 17*)		1.4 0.8 0.5	2	nC nC nC

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%.

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)				0.35 1.40	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 1 A, V_{GS} = 0			1.2	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 1 A, di/dt = 100 A/µs, V_{DD} = 20 V, T_j = 150 °C (see *Figure 18*)		32 25 1.6		ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark.

Table 7. TO-92 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.32		4.95
b	0.36		0.51
D	4.45		4.95
E	3.30		3.94
e	2.41		2.67
e1	1.14		1.40
L	12.70		15.49
R	2.16		2.41
S1	0.92		1.52
W	0.41		0.56
V		5°	

Figure 22. TO-92 drawing

